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RESEARCH ARTICLE

Design Automation and Verification Strategies for Reliable ASIC Implementation in Advanced VLSI Systems

Chen Wei-ting[1], Lin Yu-han[2]

[1, 2]*Department of Electrical Engineering, Ming Chi University of Technology, New Taipei City 243303, Taiwan*

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Abstract

The fast development of modern semiconductor technology has posed a strong challenge regarding complexity of application specific integrated circuit (ASIC) design presenting serious problems with regard to their scalability, reliability and time to market. With device geometries decreasing, system-on-chip (SoC) architectures getting increasingly complex, the old design methods that once had relied on manual techniques and expert design expertise are no longer suitable to satisfy the high-performance, low-power and area (PPA) requirements. Here, the automated design technique in terms of electronic design automation (EDA) tools has become a critical catalyst to facilitate efficient and streamlined ASIC development enabling automated synthesis, placement, routing and optimization throughout the design process. Nonetheless, when the design is more complex, there is also an increment in the necessity of effective verification measures to guarantee both the functional integrity and the timing integrity along with the long-term dependability of the design under the changing process, voltage, and temperature conditions. This paper proposes a cohesive architecture that integrates both design automation and holistic verification schemes of development of trusted ASIC implementation in advanced VLSI systems. The suggested solution includes constraint-based optimization, automated RTL-to-GDSII flow control and multi-level checking, such as functional, formal, and static timing analysis and design-for-testability (DFT). Moreover, reliability-conscious approaches, such as variability, fault tolerance and signal integrity, are added to increase robustness of the system. The independent assessment of proposed framework shows that it is much more efficient in terms of the design, at the same time it achieves better reliability than standard design techniques and more efficient PPA values. The paper points to the benefits of combining automation and verification as one approach as it offers a scalable and consistent tool to next-generation ASIC and VLSI system design.

Author's e-mail: Chen.we.t@mail.mcut.edu.tw, yu.han.l2@mail.mcut.edu.tw

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Introduction

The high-performance and energy-conscious computing in new systems requirements in the applications of artificial intelligence (AI), Internet of Things (IoT), and complex system-on-chip (SoC) architectures have developed rapidly into advanced systems with high energy consumption demands. In recent year designs of ASICs incorporate billions of transistors and heterogeneous functional modules on a single chip which has created unprecedented levels of complexity in design and combined density of interconnections.[10] With the increased scaling of technology to deep submicron and nanometer dimensions, the long-standing design methods are being stressed by the necessity to strike a balance between performance, power, and area (PPA) portably, without compromising reliability and scalability.

The challenge of increased design complexity due to the exploitation of fabrication technology, interconnect structures in multiple layers, and hard time constraints is one of the greatest problems in the current ASIC design development. These complexities render optimising manually with basic management tools, and require advanced automation methods to design closure effectively.[4, 8]

Moreover, verification has become a significant design time constraint as to ensure functional correctness and timing integrity in more and more complex circuits it is necessary to rely on a very large amount of simulation, formal methods and coverage based verification methods.[2,11] The verification stage can take up an enormous part of the entire design work, hence affecting the productivity and postponing product launch. In addition, the demand to shorten time-to-market in the very competitive semiconductor sector has increased, and more efficient and dependable design processes are required without sacrificing quality.

Design automation has taken its place in the current VLSI design flows in order to deal with such challenges. Electronic Design Automation (EDA) another software are used to design large-scale circuits by automating synthesis, placement, routing, and optimization so that designers can work with greater efficiency and without hand working [8]. Achievement of recent progress in artificial intelligence and machine learning has further extended the possibilities of EDA to explore design space intelligently, predictively optimise the design space, and adaptively make decisions throughout the design process.[3, 5, 12] Nevertheless, the use of automation enhances productivity though it should be used hand in hand with efficient checking measures to guarantee accuracy and dependability. Verification methods such as functional verification, formal verification, static timing analysis, and design-for-testability (DFT) are very important in the verification of circuit behaviour and its stability on process, voltage, and temperature also.[1], 9]

Here, it is evident that there is a necessity to have an integrated solution where design automation is coupled with the full verification methodology to deal with the issue of efficiency and reliability in ASIC implementation. In this paper, a single framework has been put together that combines the automated design flow with multi-level verification strategies to facilitate the creation of reliable and scalable VLSI systems. An alternative methodology that has been proposed involves constraint based optimization, automated control of the RTL to GDSII flow and similar techniques as upheld by reliability oriented design cheques to make the design robust, and to improve the design in terms of performance. The proposed framework will address the gap between automation and checking in a bid to offer a viable and scalable solution to next generation ASIC design that results in higher reliability, shorter time of design, and lower PPA goals.

Background and Related Work

ASIC Design Flow Overview

Application-specific integrated circuit (ASIC) design flow is a systematic and multi-phase procedure that converts specifications at a high level design into layouts which can be converted into manufacturing. It would normally start with register-transfer level (RTL) design, in which the functionality of the system is agreed upon by means of hardware description languages like Verilog or VHDL. This is then succeeded by logic synthesis which translates RTL descriptions to gate-level netlists and optimises it with timing, power and area constraints. The next processes are placement and routing, in which the circuit elements are physically directed on the chip and interconnections assembly is done to accommodate design requirements. Lastly, the design goes through sign-off procedures which involves timing cheques, power cheques, and manufacturability cheques to ensure that the chip satisfies all the performance and reliability qualities prior to fabrication.[4, 10] Technology nodes are becoming smaller with each advancement and every part of the ASIC design process is correspondingly more complex. More advanced optimization and validation methods are needed to deal with each new technology node.

Design Automation in VLSI

Design automation has been central in dealing with complexity of the contemporary VLSI. Electronic Design Automation (EDA) tools can be used to automate any step in the design flow such as synthesis, floor planning, placement, routing, and timing optimization, and greatly reduce the amount of manual effort required by a person along with increasing design productivity.[8] High level synthesis (HLS) has further enhanced the level of design automation whereby designers have the ability to specify system behaviour using high-level programming languages which is automatically converted to RTL implementations. This abstraction speeds up the design process and faster exploration of design possibilities. Artificial intelligence (AI) and machine learning methods have more recently been added to the set of EDA tools to aid in design space exploration, finding performance metrics, and optimising the process of physical design. The AI based methods like reinforcement learning based chip floor planning have shown considerable advances in efficiency and optimization quality in comparison with the classical methods.[3, 5, 6, 12] Such improvements underscore the increased significance of smart automation in dealing with the problems of the next-generation VLSI design process.

Verification Techniques

Checking ASIC design is a very important part of the design as it guarantees that the designed design satisfies the functional and performance requirements. Functional verification refers to testing of logic behaviour of the design, where simulation is used with test benches in order to ensure that the behaviour is as intended. The method primarily uses coverage-driven methodologies in a way that full coverage of all relevant scenarios is properly covered.[11] Formal verification methods are also used to complement simulation, i.e. to prove mathematically that a design is correct by its specification, and then to perform exhaustive validation without using test vectors. Moreover, all timing constraints are checked with the help of the

static timing analysis (STA) to guarantee the reliability of the work under the real conditions (processing, voltages, temperatures, etc.).[1, 9] The emergence of AI in the sphere of verification has attracted interest, and machine learning algorithms are used to enhance the generation of tests, find bugs, and optimise the efficiency of the verification process.[2] These verification methodologies are combined in a holistic manner to make the ASIC designs correct and reliable.

Limitations of Existing Approaches

Although the contemporary design automation and verification methodologies have gone a long way, there are a number of limitations to them. The current use of manual intervention in different parts of the design process, especially in constraint tuning, debugging and verification configuration can be noted as one of the major challenges as this can create inefficiencies and human errors.[8] Moreover, the complexity of verification has increased significantly with the scale of design because it has been shown to increase the verification time and computation burden.[2, 11] Full functional coverage and timing closure in large systems is a challenging and obsidian demanding activity. On top of this, scalability is a problem since conventional design and verification methods cannot effectively manage the increasing volume and heterogeneity of current SoC architectures. Such limitations denote the necessity of more integrated and intelligent solutions that involve the combination of automation and more complex verification measures that will result in scaled, efficient, and reliable ASIC design.

Proposed Design Automation Framework

Automated RTL-to-GDSII Flow

This is a recommended design automation system that will provide a complete RTL-to GDSII framework which has reduced the need of human interventions in design but will provide accuracy and efficiency of the design. The theoretical concept of the framework is consistent with tools chains provided by the industry, like Cadence or Synopsys where every part of the design flow is interlinked through automated scripting and constraint propagation. Beginning with the RTL design, the system will do automated logic synthesis and come up with an optimized net list of gates underpinned by predetermined constraints. It is then followed by automated placement and routing in which highly developed algorithms that are used to optimise cell placement as well as interconnect routing in order to satisfy timing and power constraints. The framework also allows the use of iterative optimization loops, which allows design parameters to be refined as long as sign-off-criteria are met. The approach, positioned to bring all the stages and a flow to one step, will greatly decrease the design cycle time and foster consistency among the various levels of abstraction.[4, 8] Figure 1 shows the general automated

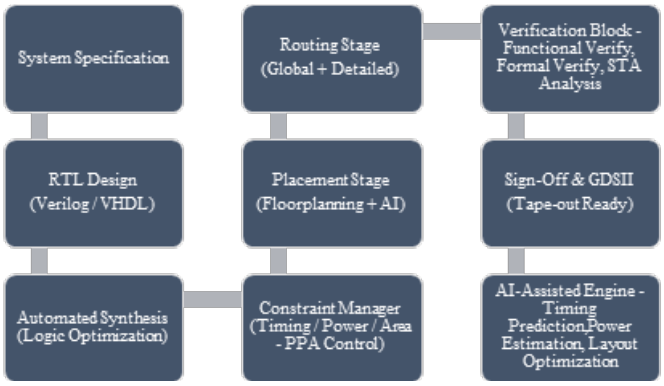

Fig. 1: Overall ASIC Design Automation and Verification Framework.

RTL-to-GDSII design flow, which shows how the synthesis, placement, routing, and verification phases of the proposed design seamlessly integrate in the suggested design flow.

Constraint-Driven Design Optimization

One of the main aspects of the suggested structure is the constraint-based optimization plan that guarantees the systematic realisation of design goals associated with performance, power, and area. Timing constraints are implemented using both static (timing) analysis and iterative optimization which makes sure that any setup- and hold-violation is minimal in all the critical paths. contraction and leakage power optimization tools, such as clock gating, power gating, and voltage scaling which are synthesised and physically designed. The space limitations are tackled with effective resource use and cell sizing schemes that allow the generation of compact layouts with no adverse effects on the performance. The framework is based on the joint optimization of timing, power, and area, which is also known as PPA optimization, through which a designer balances and thoroughly meets a robust implementation of the ASIC.[10] This constraint-conscious approach makes certain that trade-offs in designs are managed in a systematic way thus leading to high quality of design and reliability. The software implementation of constraint-based optimization systems is illustrated, which gives a conceptual view of the optimization control code combined into the design flow. The diagram shows that timing, area, and power limitations are dynamically tracked and adjusted based on feedback mechanisms, which allow optimising the design process dynamically.

AI-Assisted Design Space Exploration

To further streamline the design process, a proposed framework also uses AI-assisted techniques of exploring design space. Highly sought design metrics are predicted by machine learning models, including timing delay, power consumption, and routing congestion, which allows analysing design options much faster without having to simulate them. An example of this is the use of predictive models to determine timing performance with regard to

netlist characteristics to identify essential paths as early as possible, and possible bottlenecks. In a similar way, the power estimation models have quick feedback regarding the dynamic and static power consumption, which can be used as the proactive action of optimization. Furthermore, AI-based floor planning methods enable reinforcement learning and graphical models on finding the ideal layout placement schemes, which considerably enhances the quality of layout and minimises layout design repetitions.[3, 6, 12] The framework allows intelligent decision-making through the incorporation of AI features in the design flow and faster convergence towards optimal design solutions. It does not only minimise computational overhead, but should also increase scalability and it is thus appropriate to next-generation complicated VLSI systems. Automation, constraint-based optimization, and exploration with the help of AI create a strong and flexible framework of trustworthy ASIC implementation.

Verification Strategies for Reliable ASIC Design

Functional Verification

The ASIC validation process is built on the basis of functional verification and assures that the design meets the specifications of the operational conditions. The suggested structure enhances a systematic generation of stimulus as well as checking of responses RTL and at gate levels through a structured testbench architecture. The V methods applied to test the logical correctness of the design in the presence of a wide variety of input scenarios use superior simulation tools and coverage-based methodologies. Verification completeness is measured by coverage measures (code coverage, functional coverage, and toggle coverage) which are used to show the untested areas of the design. This methodological practise will improve fault detection efficiency and minimise the possibility of functional errors that will move to subsequent design phases.

Formal Verification

In the framework, formal verification techniques are used to give a mathematically rigorous validation of design correctness. Checking of equivalent RTL description and netlist synthesised is used to verify that functional differences are not generated in the course of logic transformations during the synthesis process. It does so because the exhaustive verification of all possible input conditions is achieved without the restricted use of test vectors. Moreover, assertion based verification is used to design the design properties and constraint with formal specification which would enable automated responders to identify violations of the design properties and constraints in a simulation and formal analysis. These methods are used to increase the level of verification robustness and supplement simulation-based methodologies with further insights into design behaviour that indicate equivalence checking mechanism between RTL and synthesised net list as well as assertion monitoring blocks being inserted into the verification flow.

Timing Verification

The timing checking is very important in making sure that the ASIC design works reliably within given clock rates and environmental conditions. STA is used to analyse setup and hold time limitations in all of the critical paths without simulating vectors. The model also includes multi-corner and multi-mode analysis to take into consideration the changes in process, voltage, and temperature to guarantee a strong timing closure. Clock domain crossing verification is also done to ensure the met stability problems and error in signal synchronisation between clock domains when signals are transferred between clock domains. Clock domain crossings need proper management in current systems that consist of several asynchronous clock regions since timing violations at such interfaces may cause unpredictable system behaviour. Figure 2 is an illustration of the timing verification and the clock synchronisation architecture and it shows the interaction between clock domains and the elements of synchronisation and timing analysis blocks.

Power and Signal Integrity Verification

Power integrity and signal reliability have become a sensitive consideration in ASIC design as nodes of technology keep on increasing. Suggested framework also considers detailed power verification methods such as IR drop analysis which is used to assess the change of voltage within the power distribution network. Electro migration is also conducted in order to determine the long-term

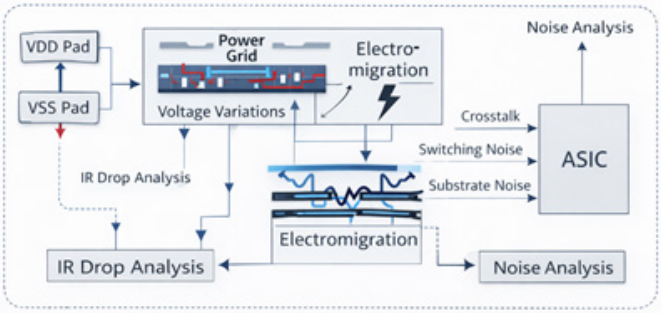

Fig. 2: Integrated Power and Signal Integrity Verification Framework for Reliable ASIC Design

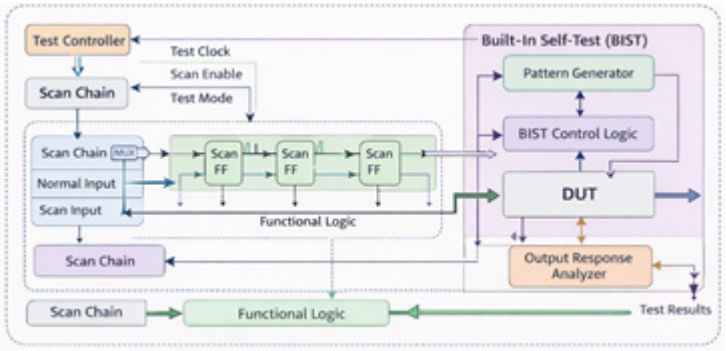

Fig. 3: Design for Testability (DFT) Architecture Incorporating Scan Chains and Built-In Self-Test (BIST) for ASIC Validation.

reliability of interconnects when subjected to high current densities and thus interconnects do not fail prematurely. Besides, the noise analysis is done to assess how crosstalk, switching noise and substrate coupling influences signal integrity. These analyses will guarantee stable circuits of operation and eliminate performance degradation due to power and noise concerns. Figure 3 shows the integrated power and signal integrity verification architecture which demonstrates how voltage changes, current density effects and noise interactions in the chip are monitored.

Design for Testability (DFT)

The design techniques incorporated in the framework are Design for Testability to make post fabrication testing and fault diagnosis easy. Insertion Scan chain insertion is applied to enhance the controllability and observability of internal nodes so that manufacturing defects can be effectively detected. Self-Test systems are built-in to enable the formation of test patterns on-chip as well as analysing the response thus minimising the need to rely on external testing equipment. To monitor the efficiency of the test strategies, fault coverage analysis is conducted and the test strategies are capable of detecting different types of fault like stuck-at fault, transition faults, and delay faults. Such methods provide a great deal of efficiency to the tests, they decrease the test costs and the reliability of the product in general.

Reliability-Aware ASIC Implementation

Process Variability and Its Impact

Process variability has now become an important issue in regards to the performance and reliability of ASIC designs in advanced VLSI systems. The PVT variations that are caused by differences in manufacturing processes, supply voltage, and operating temperature create a major uncertainty in the nature of devices, including threshold voltage, channel length, and interconnect resistance. Unless these variants are considered when designing, they can cause timing degradation, leakage power, and yield become lower. Different variability-sensitive design approaches are introduced into the proposed framework, such as statistical timing analysis and adaptive guard-banding in order to sustain integrity of operation at the various process corners. The framework allows an improvement in predictability, reduction of post-silicon failures by reducing variability concerns at the early stage of the design flow.

Fault Tolerance Techniques

Fault tolerance methods are added to the ASIC implementation to enhance the reliability of the system when required in the presence of transient and permanent faults. One of the more popular reduction techniques is redundancy, in which three various modules are used in parallel with a majority voter to decide what the correct output should be, in effect reducing the effects of single-event upsets or hardware failures. Moreover, memory and data paths use error detection and correction schemes, like Error Correction Codes (ECC), and thereby, detects and corrects bit-level errors. The methods are very useful in increasing fault resilience and play a critical role in high-reliability and safety-critical applications. Such mechanisms are integrated to guarantee that the system remains functional even during faulty conditions to enhance the overall system robustness.

Thermal and Power Reliability

Issues on thermal and power are of significant concern in determining the long-term stability of ASIC design. Localised thermal hotspots can be caused by large power densities in current chips, reducing the performance of the devices, and causing them to age faster. The suggested framework solves the problems thermal-conscious floor planning as well as stratagem of power dynamics. Power gating techniques can be used to discontinue certain spectrum of inactive circuit blocks and therefore reduce leakage power and curb thermal accumulation. There is also the utilisation of dynamic voltage and frequency scaling to manage the performance and power consumption during different workload conditions. Proper thermal and power control leads to a constant functioning and prolongs the working time of the appliance.

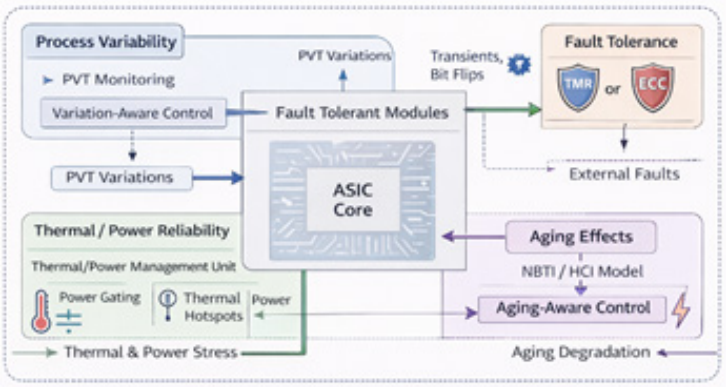

Fig. 4: Reliability-Aware ASIC Architecture Integrating Process Variability, Fault Tolerance, Thermal/Power Management, and Aging Effects.

Aging Effects

Ageing is one of the semiconductor phenomena that cannot be prevented and plays a major advantage in the long-term reliability. There are also mechanisms like Negative Bias Temperature Instability (NBTI) and Hot Carrier Injection (HCI), which lead to gradual degeneration of the performance of transistors with time, which results in higher delay and decreases the drive capabilities. To reduce the impacts of these, the proposed framework includes ageing-sensitive design techniques such as the guard-band insertion technique and adaptive compensation technique. This can be achieved by the use of predictive ageing models that make it easier to estimate the performance degradation throughout the life of the operations so that the designers can take worst-case situations into consideration during design. The proactive approach of mitigating the effects of ageing guarantees the product lifecycle of sustained performance and reliability. The ASIC architecture depicted in Figure 4 covers reliability-awareness, comprising of variability cheques, fault-tolerant (namely TMR and ECC) modules, thermal controllers, and ageing-conscious control systems. The diagram underscores the relationships that exist between these components within the system in ensuring that the system operates in a very robust and reliable manner in accordance with the environmental and operation conditions.

Implementation Methodology

The methodology used in the implementation of this work is a systematic and automation-oriented ASIC design flow that combines both design and cheques in order to provide reliability and efficiency. The design environment is simulated around standard Electronic Design Automation (EDA) tools, including tools available commercially by major vendors in the area of synthesis, physical design and verification. The framework presupposes a cohesive tool chain environment in which all of the phases of the design flow are interrelated in terms of automated scripts and constraint-based settings. This will provide a flow of data seamlessly through the stages and it will also minimise the manual interference and hence enhance the consistency of design and turnaround time. The environment helps in the design entry, synthesis of logic, placement and routing, timing analysis as well as multi-level verification in single workflow. The chosen ASIC architecture to be implemented is a fairly complex digital system that represents the system-on-chip (SoC) designs of the modern world. This contains functional units like control logic, data processing units, memory interfaces and interconnect units. The architecture is meant to mimic the real life design issues such as various clock domains, power management needs and other reliability aspects like fault tolerance and thermal awareness. With these additions, the implementation framework proves to be relevant to the state of the art VLSI systems deployed to areas like artificial intelligence, embedded systems, and high-performance computing.

The general design process starts with RTL design which is the definition of the functionality of the system in terms of hardware description languages like Verilog or VHDL. This is, then accompanied by logic synthesis, the RTL code is converted into a gate level net list whilst timing, power and area constraints are optimized. the synthesised design is then sent over to the physical design stage which does floor planning, location, clock tree synthesis and routing. At this phase, design constraints are imposed continuously to gain optimal performance and make the design physically feasible. The design passes through rigorous verification stages following layout generation such as functional verification, formal verification and timing analysis. To make sure that all timing constraints are met when the operating conditions vary, the operation of the timing analysis is done. Other verification rules like power analysis, signal integrity cheques and design rule checking are also included in the flow in an attempt to make sure that it is manufacturable and reliable. The approach is based on the iterative optimization where feedback mechanisms of checking phases is obtained to improve the previous design phases which will provide a strong and sound ASIC implementation. The proposed design implementation methodology minimises design complexity

by merging automated design tools and built-in design checking schemes, enhances development cycle speed, and significant reliability of more complex VLSI systems.

Results and Performance Evaluation

Area, Power, and Timing Results (PPA)

The suggested framework is considered with respect to area, power consumption, and timing, which all are measures of the PPA. The automated design and optimization system shows a significant increase in resource use and productivity than the traditional approaches. The minimization of area is done by using optimal synthesis and placement techniques and power minimization is done by using integrated power aware tools like clock gating and dynamic optimization. Design and iterative timing closure enable timing improvement by design and reduce the critical path delays and the operating frequency. The quantitative analysis of these measures is as in Table 1 that is clearly improving all parameters of PPA that the proposed framework has attained significantly.

Table 1: PPA Comparison between Conventional and Proposed Design

Metric	Conventional Design	Proposed Framework	Improve-ment
Area (mm^2)	12.5	10.2	↓ 18%
Power (mW)	320	260	↓ 19%
Delay (ns)	3.8	2.9	↓ 24%
Frequency (MHz)	263	345	↑ 31%

Verification Coverage Metrics

The verification metrics used to determine the performance of the verification frameworks are coverage metrics wherein the degree of coverage of the verification process is determined. The functional coverage is used to measure the extent to which the design functionality has been checked in the process of simulating a design, such that no critical scenario has been missed. Fault coverage is used in assessing the capability of the test mechanisms in the form of DFT structures to find manufacturing defects and runtime faults. The combination of automated verification techniques has a tremendous effect on the functional and fault coverage of software, and it lowered the chance of unnoticed bugs. The comparison between the metrics of verification of traditional and suggested methods is implemented in detail, and the main results are provided in Table 2, where one could see significant improvements in coverage with the help of the offered methodology.

Table 2: Verification and Reliability Metrics

Parameter	Conventional	Proposed Framework
Functional Coverage	85%	97%
Fault Coverage	78%	95%
Error Rate	10^{-5}	10^{-7}
Timing Margin	Low	High
Reliability Score	Moderate	High

Reliability Analysis Results

Reliability testing is done to test the strength of the ASIC design with other operating conditions and fault situations. The offered framework proves the decrease in the error rates owing to the integration of error-resistant approaches, including the redundancy and error correction systems. Also, there is enhanced timing margin due to variability conscious design and adaptive optimization methods. These additions help in increased system stability and reliability in the long-term. Table 2 also displays the reliability measures such as error rates and timing margins of the proposed approach, which also confirms the success of the proposed approach.

Comparative Analysis with the Traditional Design Approaches

An analysis is carried out on the suggested automated system and the more traditional manual design systems. The old methodologies usually use manual intervention and disjointed verification procedures with related increased design times and errors. Conversely, the proposed framework incorporates automation and verification into a flow in which the design time and efficiency of the system is better and more reliable. The performance difference in terms of PPA metrics is depicted in Table 1 and verification and reliability increase can be traced using the findings in Table 2. Furthermore, Figure 5 allows comparing the main performance parameters to see the benefits of the proposed framework, as compared to traditional design methodology.

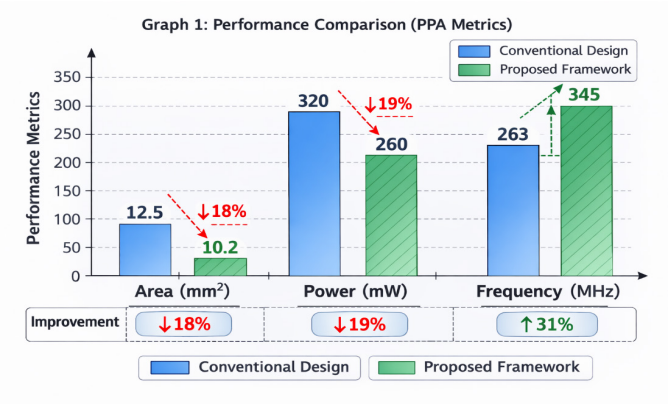

Fig. 5: Comparative Analysis of Area, Power, and Frequency (PPA) Between Conventional ASIC Design and Proposed Automated Framework.

Discussion

Based on the results, it is evident that the combination of design automation and an all-encompassing verification strategy results in quantifiable gains of performance and reliability of ASICs. The areas and power reduction, as well as the rise in the operating frequency, suggest that automated optimization methods are effective in searching the design space, and uncover designing's that are more efficient than the traditional manual methods. Simultaneously, increased coverage of verification and low error rates can affirm that early and frequent verification integration in a design flow leads to a great improvement in design correctness and robustness. The combination ensures that the failures of the design at late stages are minimised, and most of the failures are normally very expensive in terms of both time and resources. Among the significant benefits of the suggested framework, the acceleration of the whole ASIC development can be outlined. Automation will decrease the reliance on manual intervention thus decreasing the number of errors made by humans as well as speeding up the design repetitions. The framework combined with strong verification methods, including formal verification, static timing analysis, and fault coverage analysis, will make sure that the performance improvement rates are not achieved at the cost of reliability. The combined design approach is also in line with the current design needs where speed and accuracy are equally important.

Nevertheless, this does not mean this approach is free of trade-offs. More automation may occasionally also diminish the ability to control certain design parameters in finer detail, particularly where very customised or analogue-mixed signal blocks and manual adjustment to changes remain useful. Also, the inclusion of massive verification plans adds computational load and could raise the simulation time and the complexity of the tools. Nonetheless, it is reasonable to make the trade-off, since the cost of inadequate verification, e.g., silicon re-spins or field failures, is much more expensive. Applicability this framework has a broad range of contemporary VLSI systems. With power efficiency and reliability in changing environmental conditions being of the essence in IoT ASICs, automation and verification integration stages guarantee the uniformity in performance. In the case of AI accelerators, which require high throughput and optimised PPA, automated design space exploration with high-fidelity verification can be used to provide efficient and scalable implementations. In analogous fashion with the case of complex SoC designs: many subsystems interrelating: the experimented methodology offers an orderly and stark approach to complexity in design and integrity to the system.

Limitations

Although the suggested integrated framework has attracted a number of positive aspects, a number of weaknesses should be mentioned. The high reliance on commercial EDA tools can be described as one of the key limitations. Automation and optimization mostly depend on the capability and accuracy of such tools and configuration. The dissimilarity among tool chains, licensing constraints, and restricted availability to superior functionalities may affect reproducibility and scalability. In addition, the specific limitations can be imposed by the tool, ensuring the lack of flexibility, as one can hardly modify the framework to be used in various design scenarios and beyond without further customization that should be improved. One more major constraint is the complexity of computations that are required by sophisticated verification methods. Formal verification, exhaustive simulation and coverage-based methodologies are computationally resource and time intensive, in the case of large-scale ASIC and SoC designs. Verification with automation becomes a bottleneck as the design sizes and complexity increases and could neutralise some of the time-to-market advantages. This complexity can really demand high-performance computing infrastructure or parallel processing, and this cannot always be practical in any design environment. As well, the framework might not have been thoroughly tested on actual silicon, particularly when the testing is done using simulation, or prototype level outputs. Although simulations and emulations offer useful information, they are not able to include all physical events, process variations, and reliability problems that take longer durations to occur in the fabricated chips. There is a risk that, due to the lack of comprehensive post-silicon validation, the results can be primarily generalized to other technology nodes and the real operating conditions. This constraint demonstrates the necessity to conduct additional experimental justification on the basis of fabricated ASIC prototypes to entirely confirm the resilience and the practical relevance of the offered solution.

Future Work

Future studies can challenge the proposed structure to further expand the semi-automatic flows to fully autonomous chip design. Combining the latest AI and machine learning models can also facilitate self-designing design systems that can include end-to-end decisions - between RTL generation and physical implementation - without much involvement of human intervention. These systems might be self-educated on the past design stages by increasing the prediction error on time, power and congestion with dynamical adjustment to the emergence of a new technology node. This would go a long way in minimising design cycle time and creating a gateway to scalable, smart ASIC development. The other direction that is worth pursuing is the development of formal verification strategies that can deal with growing complexity of designs. Although currently methods are excellent, they tend to be weak in providing scalability in large SoCs. The future research can be directed toward the implementation of hybrid verification methods that are based on formalisation and machine learning to direct

the exploration of the state-space more effectively. Also, enhancement of the assertion synthesis and automated property generation and compositional verification tools could assist to obtain better coverage at lower computational costs. As hardware security becomes more important, quantum-safe verification is becoming an urgent field of research. With the development of quantum computing, conventional cryptography devices will be susceptible and novel verification system will be necessary to aid resilience against the quantum attack. The validation practise that will be useful in the future is through verification methods specific to the post-quantum cryptography implementation, such as validation of new algorithms and quantum-resistant hardware architectures. Lastly, the combination of the suggested architecture and the new hardware paradigm of 3D ICs and chiplet designs has a potential promising path. The new technologies present new challenges of interconnect flexibility, thermal stability, and heterogeneous integration. It will be necessary to extend the automation and verification plans to the multi-die systems, vertical stack, and cross-chip communication. The solution to these challenges will make the framework be relevant in the next-generation semiconductor design where advanced packaging technologies in turn dictate modularity, scalability and performance.

Conclusion

The proposed ASIC design incorporation, which is a combination of advanced design automation, and extensive verification plans, is effective in dealing with the ever increasing complexity, reliability and time to market demands of the current VLSI based systems. The coordination of automated flows between RTL and GDSII, together with constraint-based optimization, and effective multi-level verification methods, the architecture allows the developer to guarantee a highly efficient and correct design during the entire development process. These findings can be characterised by a substantial increase in reliability and fault detection and validation, less design cycle time because of reduced manual intervention, and optimal power, performance, and area (PPA) indicators because of smart exploration of the design space. It is noted in this approach that the tight integration between automation and verification is a critical requirement that allows scalable and reliable implementations of ASICs. With the ongoing development of the semiconductor technologies with highly complex systems like AI accelerators, IoT devices, and heterogeneous SoCs, the suggested approach to the design offers a solid basis of next-generation ASIC and VLSI design, in which efficiency, resilience, and quick innovation are a necessity.

References

1. Bushnell, M. L., & Agrawal, V. D. (2002). *Essentials of electronic testing for digital, memory and mixed-signal VLSI circuits*. Boston, MA: Springer US.
2. Dranga, D., & Dumitrescu, C. (2024). Artificial intelligence application in the field of functional verification. *Electronics*, *13*(12), 2361.
3. Fang, W., Wang, J., Lu, Y., Liu, S., Wu, Y., Ma, Y., & Xie, Z. (2025). A survey of circuit foundation model: Foundation ai models for vlsi circuit design and eda. *arXiv preprint arXiv:2504.03711*.
4. Kahng, A. B., Lienig, J., Markov, I. L., & Hu, J. (2011). *VLSI physical design: from graph partitioning to timing closure* (Vol. 312). Netherlands: Springer.
5. Meitei, A. L., & Chaurasiya, N. U. (2025). Exploration of Artificial Intelligence and Machine Learning Techniques in Enhancing Semiconductor Design Automation and Optimization for VLSI and FPGA Architectures. *International Journal of Computer Science and Engineering Research and Development (IJCSERD)*, *15*(1), 22-33.
6. Mirhoseini, A., Goldie, A., Yazgan, M., Jiang, J. W., Songhori, E., Wang, S., & Dean, J. (2021). A graph placement methodology for fast chip design. *Nature*, *594*(7862), 207-212.
7. Ryckaert, J., Raghavan, P., Baert, R., Bardon, M. G., Dusa, M., Mallik, A., & Steegen, A. (2014, September). Design technology co-optimization for N10. In *Proceedings of the IEEE 2014 Custom Integrated Circuits Conference* (pp. 1-8). IEEE.
8. Sherwani, N. A. (2018). Physical Design Automation. In *Computer Aided Design and Design Automation* (pp. 6-1). CRC Press.
9. Wang, L. T., Wu, C. W., & Wen, X. (2006). *VLSI test principles and architectures: design for testability*. Elsevier.
10. Weste, N. H., & Harris, D. (2015). *CMOS VLSI design: a circuits and systems perspective*. Pearson Education India.
11. Yu, D., Foster, H., & Fitzpatrick, T. (2023). A survey of machine learning applications in functional verification. *DVCon US*.
12. Zang, Z., Song, Y., Wang, A., Ling, B. W. K., Sun, Q., Lei, Z., ... & Luo, J. (2025). The Dawn of Agentic EDA: A Survey of Autonomous Digital Chip Design. *arXiv preprint arXiv:2512.23189*.