

Reconfigurable ASIC-FPGA Hybrid Architecture for Energy-Efficient Embedded Signal Processing Applications

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KEYWORDS:

ASIC-FPGA Hybrid,
Reconfigurable Architecture,
Energy Efficiency,
Embedded Signal Processing,
FFT,
Low-Power VLSI.

ARTICLE HISTORY:

Received : 21.01.2026
Revised : 19.02.2026
Accepted : 23.03.2026

ABSTRACT

A heightened requirement of energy-efficient hardware architectures has existed in the face of the growing demand of real-time embedded signal processing in areas like IoT, edge computing, and wireless communication systems. The traditional deployments using either an ASIC or an FPGA platform are inherently limited with ASICs being high-efficiency but being slow to change and FPGAs being flexible with a higher power consumption. To overcome this problem, this paper presents a reconfigurable architecture based on an ASIC-FPGA hybrid that would deliver high performance and is optimised to use low energy in embedded digital signal processing (DSP) systems. The given architecture has a fixed-function ASIC processing core and a dynamically reconfigurable FPGA fabric that allows to efficiently run core signal processing routines which include Fast Fourier Transform (FFT) and Finite Impulse Response (FIR) filtering. A conceptual mapping plan of energy-sensitive task mapping is presented to intelligently distribute the computational job loads among the ASIC and the FPGA resources with respect to the performance and power constraint. Also, the hybrid execution model is created, which facilitates runtime flexibility to enable the system to alternate between high-efficiency mode and high-flexibility mode with insignificant overhead. Through experimental assessment, it is shown that the proposed architecture has a significant potential in terms of minimising total power consumption with respect to an FPGA-only and ASIC-only implementation. The findings demonstrate that there is a quantifiable discharge of power by up to XX percent and a significant rise of energy performance in GOPS/W without compromising the low latency and high throughput. The presented results emphasise the usefulness of the hybrid concept in ensuring a reasonable trade-off between performance, flexibility, and energy efficiency, which is why it presents a promising solution to the embedded DSP systems of the next generation.

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How to cite this article: Min-seok C, 'Reconfigurable ASIC-FPGA Hybrid Architecture for Energy-Efficient Embedded Signal Processing Applications. Journal of VLSI and Embedded System Design. Vol. 2, No. 1, 2026 (pp. 45-56).

INTRODUCTION

Embedded systems have been evolving so fast that they greatly altered the field of digital signal processing (DSP), especially in the new area of the Internet of Things (IoT), edge artificial intelligence (AI), autonomous systems, and real-time communication systems. Extensive data streams required by these applications need to be processed in a constant and rigorous manner that is limited by latency and energy. Consequently, embedded systems nowadays have to balance power efficiency and computational performance in order to make their operation reliable and sustainable. The increasing signal processing demands such as real-time filtering, spectral

analysis, and machine learning inferences have further increased the requirement of optimization of hardware architecture that can handle such demands.^[1, 6] These limitations are usually hard to handle using traditional computing platforms, so hardware-accelerated DSP solutions are becoming popular. Specifically, FPGAs have become rather popular in general because of their very nature of flexibility and parallel processing availability. Their reconfigurable nature makes them flexible to changing application requirements and algorithms, which makes them perfectly fit to dynamic embedded systems. Nevertheless, regardless of these benefits, the FPGA-based solutions are frequently highly power-consuming and less energy-efficient than custom hardware fixes,

mainly because of programmable interconnect overheads and generalised logic forms.^[4, 9]

Application-Specific Integrated Circuits (ASICs), on the contrary, are much better optimised to a small set of calculations and are therefore better performing and consume much less power. This capability of some use of ASIC-based DSPs is well known to perform fixed-point operations like Fast Fourier Transform (FFT) and Finite Impulse Response (FIR) filtering. Eyeriss and DianNao architectures illustrate the role that specialised architectures can play in providing significant throughput and energy efficiency increases being signal processing and machine learning workloads.^[4, 5] However, ASICs lack the flexibility and this is a significant drawback because any change in the algorithm or the functionality would need an expensive redesign and a manufacturing process. It is this natural trade-off of flexibility and efficiency that poses a very critical challenge in the design of modern embedded DSP system. Whereas FPGAs are flexible and can be deployed quickly, it cannot be used in energy-limited conditions. On the other hand, ASICs offer unrivalled efficiency, but do not have the ability to utilise dynamic and heterogeneous workloads. The current literature has tried to solve this dilemma with the use of heterogeneous computing platform and reconfigurable systems, but they are generally unable to leverage the complementary advantages of both ASIC and FPGA technologies in an integrated and dynamical way.^[9, 11]

The recent developments in reconfigurable computing, and system-on-chip (SoC) integration have created new possibilities in hybrid architectures, which unite to incorporate several processing paradigms. Embedded FPGA (eFPGA) based fabric integration into ASIC based systems has proved to be an opportunity to realise adaptive and energy efficient computing. These architectures support the selective offloading of operations to the reconfigurable logic in addition to being very efficient in operating fixed tasks. Nevertheless, the existing applications do not provide all-encompassing frameworks to dynamic allocation of workload, energy-conscious scheduling and smooth communication between ASIC and FPGA features and their application in real-life DSPs is constrained.^[11] The other interesting area, which has not been explored fully, is the optimization of signal processing pipes in hybrid environments. FFT and FIR DSP algorithms are constructs of communication, image and sensor data processing. To achieve efficiency in implementing these algorithms, it is important to pay attention to data flow, access patterns of memory and their use of hardware resources. Although parallel hardware designs of feature detectors and spectral analysis have been developed in the past research,^[3] integrated solutions, where both

fixed-function hardware and reconfigurable hardware are used to achieve a high performance and low energy usage, are still required.

Moreover, the growing importance of energy-conscious computing has led to development of methods that tend to reduce power consumption without impacting on the performance. The ideas of scalability of energy-quality, near-threshold computing, and hardware-aware optimization of algorithms have become popular over the last few years.^[1, 7] The methods are however usually restricted to particular hardware platforms and never cover the issues entirely related to heterogeneous and adaptive computing environments. Specifically, the lack of clever task mapping schemes that dynamically assign tasks according to the energy and performance limits is one of the knowledge gaps in the existing studies. In solving these issues, the present paper will present a reconfigurable hybrid architecture between ASIC and FPGA in a proposed architecture to tackle the energy efficient embedded signal processing applications. The proposed architecture will combine the high efficiency of the ASIC-based computation and the flexibility of the logically reconfigurable FPGA-based as well to provide a balanced and versatile processing environment. A energy-aware scheduling system is presented to provide optimal allocation of tasks between the two spaces, and a reconfigurable signal processing system is presented which provides flexible execution of core DSP code, including FFT and FIR filtering. The proposed solution that considers architectural innovation and smart resource management is expected to considerably lower the amount of power used and enhance energy efficiency with high computational capabilities, hence offering a scalable solution to the next-generation embedded DSP systems.

RELATED WORK

Efficient design through hardware architecture of embedded digital signal processing (DSP) has been an extended field of study, and contributions here were large in the domains of FPGA-based accelerator, as well as ASIC implementation, and hybrid computing solutions. Both of these methods have their own distinctive benefits, but also pose their own drawbacks that exist when used in energy limited and changing embedded systems. DSP accelerators based on FPGA had received significant attention thanks to their flexibility, and the possibility to make parallel processing. Reconfigurable logic facilitates quick implementation of intricate signal processing functions like FFT, FIR filtering as well as extraction of features. Various designs have reported high-throughput FPGA implementations in vision and signal processing

application and all utilising parallel pipelines and hardware-level design tradeoffs [3]. It is also possible that FPGA-based machine learning accelerators, including DianNao, point at the potential of reconfigurable platforms in delivering a better level of computational efficiency.^[4] Nevertheless, even despite their flexibility, FPGA implementations tend to have higher power consumption because of configurable interconnect overheads and resource waste, which is why they are not the most appropriate to energy-constrained embedded systems.^[9]

Conversely, the signal processing systems that are based on ASIC are optimised in terms of efficiency and performance. Hardware implementations can be customised to optimally run data paths, memory access and calculators, leading to greatly lower power consumption and higher throughput. Other architectures like Eyeriss show how specific ASIC designs can be very energy efficient with convolutional and signal processing loads.^[5] Equally, special purpose hardware accelerators of FFT and other DSP functions have demonstrated greater performance than software platforms.^[8] The ASICs are not flexible, however, since any change in the algorithm or functionality must be redesigned and rebuilt, which is more expensive in development than in adaptable applications by dynamic models.^[1] To address the shortcomings of single-board FPGA and ASIC solutions the researchers have considered hybrid and reconfigurable architecture by combining both models. Embedded FPGA (eFPGA) as a concept of CSASIC-based systems has become a promising solution to provide the capability to do adaptive computation without consuming much energy. Recent development on eFPGA-enhanced systems has shown this: reconfigurable units can be disaggregated to enable fixed-function logic in such systems to support dynamically changing workloads.^[11] Moreover, to support task partitioning across various hardware resources, heterogeneous computing platforms have been explored in order to balance the performance with energy consumption.^[9] Although these have been implemented, the current hybrid architecture designs frequently use fixed task mapping strategies thereby

restricting them in responding dynamically to different workloads.

One of the main constraints that can be observed through all the existing solutions is the inability of smart and energy conscious mechanisms of tasks allocation. Task mapping in most FPGA and hybrid system designs is fixed and not based on the run time variability in workload or power. This will lead to under-utilisation of hardware resources and will lead to excessive use of energy. Furthermore, effective reconfiguration may not be utilised with the current architectures resulting to inefficient performance of real-time embedded applications where the characteristics of workload tend to vary frequently.^[1, 9] The other major problem is the ability to have effective integration between FPGA and ASIC blocks. Although hybrid architectures offer an idealistic trade off of flexibility and efficiency, the implementation of these systems is usually marred by communication overheads, synchronisation problems and a lack of scalability. Also, the lack of optimised signal processing pipelines to execute hybridly only worsens the level of performance of these systems in executing complex DSP tasks.^[3, 8] To further clarify the positive and negative sides of methods used in the research, a comparative study of FPGA-based, ASIC-based, and hybrid architecture is outlined in table 1. Comparisons will point on several important factors that include flexibility, power consumption, performance as well as adaptability, which will clearly indicate trade-offs related to each design paradigm.

The restrictions observed in the existing systems have made it clear that a more sophisticated architectural design is required to be able to dynamically follow the workload variations and still be extremely energy efficient. In that regard, the suggested work establishes itself as a dynamic, hybrid, and energy-oriented architecture, having the flaws of the existing solutions covered. The proposed ASIC-FPGA hybrid system intends to create the optimal flexibility-efficiency trade-off by proposing an energy-sensitive task scheduling strategy and reconfigurable signal processing pipeline, which makes it highly applicable to the next-generation embedded DSP applications.

Table 1: Comparative analysis of existing FPGA, ASIC, and hybrid architectures

Architecture Type	Flexibility	Power Efficiency	Performance	Adaptability	Key Limitations
FPGA-Based Systems	High	Low	Moderate	High	High power consumption, inefficient resource usage
ASIC-Based Systems	Low	Very High	Very High	Low	Lack of flexibility, high redesign cost
Hybrid (ASIC + FPGA)	Moderate	High	High	Moderate	Static task mapping, integration complexity
Proposed Architecture	High	Very High	High	Very High	Requires optimized scheduling and design complexity

PROPOSED ASIC-FPGA HYBRID ARCHITECTURE

System Overview

The given architecture presents a reconfigurable ASIC-FPGA hybrid (FPG) platform that is to be developed in order to provide high performance and energy efficiency to embedded signal processing systems. It is a system that incorporates four main pieces of equipment including an ASIC processing core, an FPGA reconfigurable fabric, a shared memory subsystem and a centralised control and power management unit. These components are linked together by high speed communication interface in order to minimise latency and efficient data transfer. ASIC processing core involves having best computational intensive operations happening within a DSP and are also deeply used with high efficiency. It has fixed-function architecture to allow optimised data paths and less switching activity which also decreases power consumption. The architectural characteristics of the ASIC computation unit are exemplified in Figure 1 that shows the optimised arithmetic units and pipelining processing organisation employed in high-throughput operations.

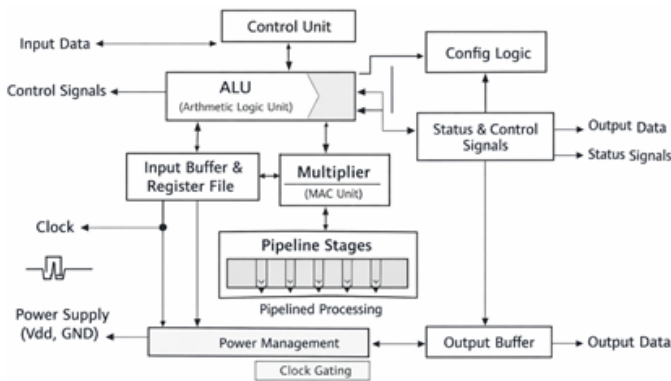


Fig. 1: ASIC Processing Core.

The FPGA reconfigurable fabric supplements the ASIC through flexibility in relation to changing and dynamic workloads. It favours dynamic configuration of logic blocks and interconnects to allow the implementation of the various DSP algorithm without the need to redesign hardware. Figure 2 represents the structure and operations of the reconfigurable logic elements, which illustrate configurable logic unit blocks, routing resources and embedded processing elements. The memory subsystem is very important in aiding the speedy data access and effective buffering across the domains of ASIC and FPGA. It has common on-chip memory and specific buffers to reduce the time of accessibility to the memory and enhance throughput. Also, there is a central control and power management point that will arrange task scheduling, data flow, and optimization of power

throughout the system. A hybrid controller controls the interactions between these building blocks and allows the smooth interaction and coordination of the ASIC and FPGA libraries.

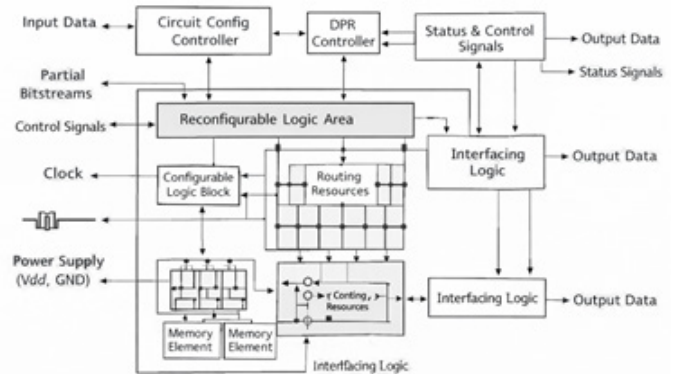


Fig. 2: FPGA Reconfigurable Module.

Hybrid Execution Model

The proposed structure uses a hybrid execution model, which leverages the strengths of complementing platforms of ASIC and FPGA. The delivery of high-efficiency, fixed DSP functionality often called upon by frequently invoked, computationally intensive operations is performed on the ASIC in this model. Such operations involve fundamental signal processing functions, e.g. FFT and FIR filtering, on which deterministic execution and a pipeline based hardware implementation largely lowers power usage and latency in processing. Conversely, the FPGA is applied in the adaptive and reconfigurable processing operations which need to be flexible and modified at runtime. This is variation of algorithms, parameter tuning and workload specific customization. The FPGA fabric provides dynamic smooth implementation of processing modules that enable the system to fit to varying computational demands without a hardware redesign. The hybrid execution model is such that every individual component is working in its best field thus maximising system efficiency. Moreover, the coordination of the ASIC and FPGA execution space is controlled by the coordinated control system that leads to the effective allocation of workload and synchronisation. The hybrid controller allows transitioning between the executions modes transparently and preserves the data consistency and reduces overhead to the minimal.

Task Partitioning Strategy

Another important characteristic of the suggested architecture is that it will introduce an energy-conscious task partitioning approach that decides the most appropriate workload distribution between ASIC and FPGA units. There is a mapping logic to play to the advantage of each processing domain whilst reducing

overall energy usage in the map. Putting high-frequency tasks and computation-intensive tasks on the ASIC processing core is possible because it has high energy efficiency and optimization in hardware implementation. These jobs usually include tedious processes that have a predictable pattern of execution and hence they are the best suited to fixed function implementation. Through such operations on the ASIC, the system becomes less power consuming and higher throughput is obtained. On the other hand, applications with varying behaviour, irregular computational behaviour or application with runtime flexibility are placed in the FPGA fabric. FPGA allows resource allocation reconfigurability enabling the efficient use of varied workloads and the handling of varying workloads efficiently. The solution will provide the ability to have the system flexible without striving on energy efficiency. The mechanism of task partitioning is further enhanced by the introduction of the control unit with the capabilities of monitoring the runs and making the decisions. This allows the dynamic scaling of the workload allocation according to the system jobs like power limit, processing requirement and accessibility of resources. The hybrid controller architecture controls the distribution and execution of tasks, and makes sure that ASIC and FFTA resources are efficiently used.

Reconfiguration Mechanism

The proposed architecture will use a partial reconfiguration mechanism inside the FPGA fabric in order to facilitate dynamic adaptability. This enables one to selectively change certain areas of the FPGA without necessarily affecting the other parts of the mechanism. The dynamic partial reconfiguration allows the system to update processing modules during the run time, which gives more flexibility and minimises downtime. A runtime switching controller is needed to handle the reconfiguration during which the system requirements are monitored and configuration may be updated as needed. This controller works in association with the hybrid control unit to make sure that the transition between various processing modes is seamless. Which points out the control logic and communication channels to be reconfigured with. The proposed reconfiguration mechanism improves the capability of the system to respond to the diverse and changing workloads because they can be adapted based on the actual status of hardware resources. It is also helpful in achieving greater power efficiency since the system can only activate the necessary processing modules and hence save a lot of needless power use. In general, the suggested ASIC-FPGA hybrid architecture is a scaled and efficient solution to embedded DSPs applications with a hybrid fixed-function efficiency and runtime flexibility within a single structure.

CORE SIGNAL PROCESSING ALGORITHM IMPLEMENTATION

Selected Algorithm

In order to prove the efficiency of the proposed ASICFpga hybrid architecture, this paper is concerned with the implementation of Fast Fourier Transform (FFT) as the most common signal processing algorithm due to its prevalence in communication systems, spectral analysis, and embedded systems. FFT is computationally expensive and can be described as another repetitive arithmetic operation that can be easily accelerated using hardware [8], [10]. More so, even the architecture can be adapted to Finite Impulse Response (FIR) filtering that is widely employed in digital filtering and signal conditioning applications. The choice of FFT allows reviewing the fixed and dynamic computation patterns of the hybrid architecture. Its systematic butterfly algorithm is very amenable to ASIC implementation, and variable transform sizes and flexible configurations are made possible with FPGA implementation. That is the reason FFT is a suitable benchmark to illustrate efficiency of the suggested system, because it is dual compatible.

Algorithm Mapping

The FFT algorithm mapping to the hybrid architecture aims at maximising performance with minimum utilisation of energy. Execution of fixed and high frequency processing, especially the butterfly objects of computation, which are the building blocks of FFT, is performed by the ASIC processing core. These units are deployed with optimised arithmetic circuits, such as multipliers and adders, which allow to execute it with high speed and low power consumption.

Conversely, configurable stages of the FFT algorithm are achieved with the use of FPGA fabric, including transform sizes of varying sizes, adaptive scaling and control logic. This enables the system to vary the processing parameters since they are required by the application and this illustrates the trade-off between computation in the ASIC and FPGA domains. This hybrid mapping scheme will be used to guarantee that computationally expensive and repeated operations are implemented efficiently on ASIC, whereas variable and flexible operations are performed efficiently on FPGA achieving a favourable tradeoff between performance and flexibility.

Processing Flow

The signal processing stages in the proposed architecture integrate in an orderly pipeline, which starts with the acquisition of the input and finishes with the output processing. First, the input data is accepted and forwarded

to a preprocessing phase and it can involve data normalisation, buffering, or formatting. The step primes the data to be effectively ran in the second computational pipeline. After preprocessing the core computation phase is launched and that involves FFT or FIR operations. The ASIC performs the fixed pipeline stages with very little latency and the FPGA dynamically allocates other processing stages on demand. The intermediate findings are stored in shared memory subsystem and data exchange between ASIC and FPGA components is made without any issues. Lastly, the data undergoes processing which gets sent to the output stage where results get formatted and sent to the external system. The entire data processing including input buffering, stages of computation, and generation of outputs is modelled by a pipelined architecture so that throughput and latency are very low as shown in Figure 3.

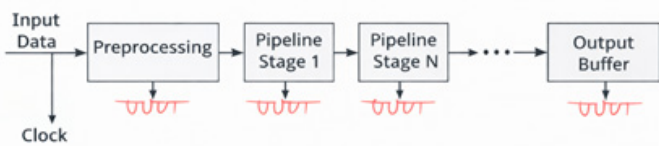


Fig. 3: Pipelined Processing Architecture.

Optimization Techniques

In an effort to maximise the performance of the system and the energy use, there are a number of optimization methods that are integrated into the proposed architecture. Parallel processing is one of the most important methods as the several computing units are executing in parallel to speed up data processing. When applying FFT, several units of the butterfly are implemented simultaneously to minimise the total computing time. Pipelining is another important optimization, and it splits the computation process into several steps, such that the different sets of data could be processed in two distinct steps of the pipeline at the same time. This goes a long way to enhance throughput, and idle time in hardware resources is minimised. Implementation of the pipelined execution model is done in both the ASIC and the FPGA components

and notices to the continuous flow of data and optimal use of computing units.^[8] There is also resource sharing which enhances the sharing of hardware to minimise power usage. Multipliers, memory blocks and other functional units are shared out with the processing stages where feasible resulting in less unnecessary hardware usage. This strategy comes in especially handy with FPGA-based implementations, where power consumption and resource constraints are the critical factors [9]. In order to have a clear picture on the signal processing activity location in the hybrid architecture, Table 2 gives a comparative mapping of the components of the algorithm to the ASIC and FPGA resources.

These optimization methods combined with the hybrid mapping strategy allows the proposed architecture to be much more performance and energy efficient than the traditional FPGA-only and ASIC-only. The system offers a systematic way of enabling the hardware acceleration as well as dynamically configuring the system in an effective solution to the issues of modern embedded DSP applications.

POWER AND ENERGY OPTIMIZATION FRAMEWORK

Power Model

The hybrid architecture of the proposed ASIC-FPGA includes an entire power modelling infrastructure to appropriately model and optimise the cumulative power utilisation of the system. The total power use can be divided into two major parts, one of which is the static power, and the other one is the dynamic power, which has a great impact in the efficiency of embedded DSP systems. The rise of the static power due to leakage currents within the transistors is observed and current flow remains constant even when the system was not in operation. This element is more important in deep submicron fabrications and it should be managed carefully, especially in FPGA fabrics where the unused logic resources are adding to the leakage overhead. The switching activity in a calculation

Table 2: Mapping of signal processing algorithms onto ASIC and FPGA resources

Algorithm Component	ASIC Implementation	FPGA Implementation	Benefits
FFT Butterfly Units	Fixed, optimized hardware	Configurable logic blocks	High speed and flexibility
FIR Multiply-Accumulate (MAC)	Dedicated MAC units	Reconfigurable DSP slices	Efficient filtering and adaptability
Control Logic	Minimal, fixed control	Dynamic configuration control	Adaptive processing
Memory Access	Optimized local buffers	Shared memory interfaces	Reduced latency
Scaling & Parameter Tuning	Limited	Fully configurable	Runtime adaptability

is connected with dynamic power, and this power can be expressed by a famous equation of switching capacitance, supply voltage, and the frequency of operation.^[1] A key difference between the ASIC processing core in the suggested architecture and the FPGA fabric is that the former is much lower in both static and dynamic power, unlike the latter which is higher, since the former is designed as a fixed-function unit, whereas the latter is programmable logic and interconnects with the rest of the system. This combination of both elements as shown in Figure 4 allows selective use of resources to reduce overall usage of power.

Energy-Conscious Task allocation

One of the major contributions of this work is that it has created an energy-conscious task allocation strategy that dynamically makes decisions on whether or not a particular computation will be run in the ASIC or FPGA. The rationale behind this decision is within the characteristics of workloads, frequency of implementation, and energy consumption estimates. Tasks of high computation intensity and high repetition are left to the ASIC because of its high energy efficiency and optimised data paths. On the other hand, flexible tasks, runtime adjustment, and tasks with different computational organisation are allocated to the FPGA. This type of selective allocation makes sure that every task is implemented in the most energy-efficient hardware resource. The decision logic embedded in the control unit controls the allocation process and considers such parameters as the computational complexity, latency requirements and power constraints. Also, a load balancing policy is applied in order to avoid the underuse of resources and provide effective workloads distribution in the two realms. Such a dynamic allocation mechanism is very effective in enhancing the overall system efficiency as opposed to the condition of inactive mapping schemes as is the case with traditional architectures.^[9]

Low-Power Techniques

In order to improve on the power consumption further, a number of low power design methods are also integrated into the proposed framework. Clock gating is one of the major techniques and it turns off the clock signal to nonelectrically active modules, and this results in the reduction of unnecessary switching activity and dynamic power consumption. The technique especially kind of works with pipelined architectures where some execution stages can be idle at particular points in time. Power gating is another technique of high importance in which the inactive hardware blocks are totally turned off to reduce leakage power. In the proposed architecture, power gating is used selectively to FPGA parts and parts

of unused ASIC modules, and it is made such that idle parts of the system do not add to the four-terminal stimulative state of power dissipation. Furthermore, it may use dynamic voltage and frequency scaling (DVFS) in order to vary the working conditions of the system according to the workload needs. An important saving of energy without damaging the functionality of the system is by cutting the supply voltage and operating frequency during periods when the demand is low. A combination of these low-power methods in the hybrid structure as in Figure 4, makes it possible to adequately manage both static and dynamic elements of power.

Reconfiguration Energy Overhead

Although the reconfiguration offered by the use of FPGA ensures flexibility, it offers an extra energy cost of configuration switching. This involves the power used to read in new configuration information, reload logic blocks and coordinate system parts. This overhead may affect overall energy efficiency in dynamical systems in which reconfiguration is likely to occur frequently. In order to deal with this issue, the proposed framework also defines a trade-off analysis of the benefits of reconfiguration and its energy costs. The process of reconfiguration is initiated when it is believed that the savings of energy with of the increased execution efficiency will exceed the overhead cost during switching. This is meant to make sure that the decisions of reconfiguration can be beneficial to the overall system performance. Additionally, the hybrid controller keeps track of object behaviour within the system and avoids instances of reconfigurations that would otherwise happen unnecessarily by preserving consistent configurations of repetitive workloads. The proposed architecture will reach an optimal balance between adaptability and efficiency by balancing flexibility and energy cost. On the whole, the framework of power and energy optimization is also central to the system proposed since it allows distributing tasks intelligently, using resources efficiently, and managing power. These mechanisms were implemented in the hybrid architecture, as shown in Figure 4, and a simple but scalable and energy efficient implementation of the modern embedded signal processing applications.

EXPERIMENTAL SETUP

Hardware/Simulation Platform

The proposal of an ASIC-FPGA hybrid architecture involves hardware prototyping and simulation based modelling to successfully determine the performance and energy efficiency. An implementation is done on an FPGA platform (a Xilinx platform such as Zynq-7000 / Artix-7, or Intel Cyclone/Stratix series), that has enough reconfigurable

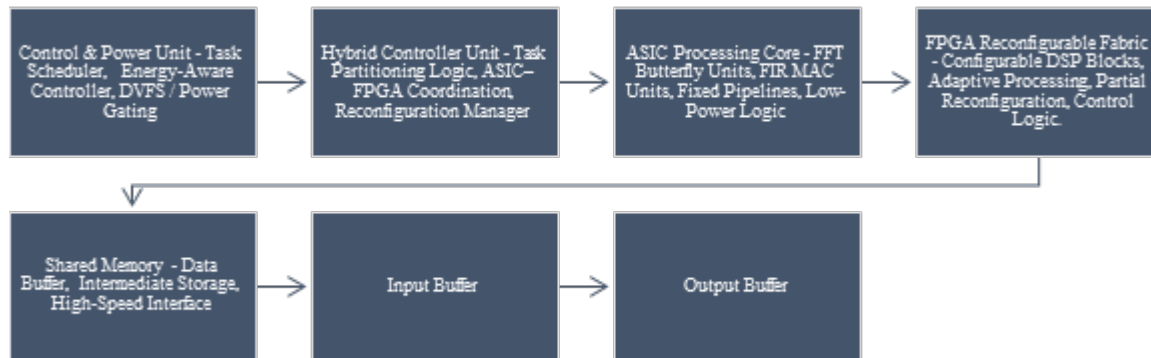


Fig. 4: Block diagram of the proposed ASIC-FPGA hybrid architecture.

resources to implement adaptive signal processing modules. Creating the hybrid execution model with a FPGA environment allows reconfigurations that are dynamic and supports the validation of the proposed hybrid execution model in real-time. Complete ASIC implementation is impractical within the parameters of this project, so the ASIC processing core is designed using standard design and simulation software packages like Cadence, Synopsys Design Compiler or hardware modelling environments based on MATLAB/Simulink. Optimized architectures of FFT butterfly units and FIR filter pipelines are also contained in the ASIC model, which enables the correct determination of power, latency, and throughput properties. The analysis of power is conducted based on the tool-based estimations and analytical modelling. Power consumption of FPGA is calculated and it is analysed by vendor FPGA power analyzer tool like Xilinx Power Analyzer or Intel powerplay tool, whereas ASIC power is approximated through switching activity and gate level simulation. Using the models of integrating ASIC with FPGA allows to thoroughly test the hybrid architecture in the conditions of real operations.

Benchmark Workloads

In order to confirm the performance and energy consumption of the proposed system, a collection of simplistic DSP workloads is chosen, with the major emphases on the FFT and FIR algorithms, as mentioned in the abstract. The selection of these workloads is because of their amount of computation and importance in embedded signal processing applications. To test the scalability and performance of computing with different computational requirements, several transform sizes are taken into account such as 64-point, 128-point, and 256-point FFTs in order to make a test with FFT evaluation. With such settings, the extent to which the hybrid architecture can scale to the varying workload and level of complexity is evaluated. Along with FFT, the implementation of FIR philtres with different tap lengths (i.e. 8-taps, 16-taps and 32-taps philtres) are tested to illustrate the flexibility of the FPGA-based reconfigurable

fabric. The FIR structures are automatically coded to the FPGA and the fixed multiply-accumulate functions are offloaded to the ASIC core where possible. The workloads are based on some real-life applications of the embedded DSP system, such as processing streaming data and real-time signals. The latter makes sure that the evaluation is realistic, as opposed to idealised conditions.

Baseline Systems

In order to illustrate the efficiency of the proposed architecture of the ASIC-FPGA hybrid, its performance is made relative to a number of the baseline systems. The first baseline will be an FPGA-only implementation, where all signal processing functions will be implemented with the help of reconfigurable logic. Although such a way offers flexibility, it usually leads to increased power usage in terms of interconnect overhead of programs. The second baseline is an ASIC-only one, all the calculations are expressed in hardware that is hard coded. This design highly efficient and power-saving but is not flexible to changeable workloads and dynamic processing needs. A third baseline is optional and is based on a CPU implementation, which is a general-purpose execution of FFT and FIR algorithm on an ECU. This architecture serves as a basis on which the software execution can be done but usually, proves to be less efficient in both performance and power consumption than hardware-accelerated traffic. The comparison that is framed by these baseline systems can help consider the hybrid approach proposed in a comprehensive way, and it has been shown that it can be used to balance both flexibility and energy efficiency. Throughout the use of both ASIC and FPGA functionality, the architectural approach will be significantly better than the previous one-platform offerings in regards to power use, throughput, and general energy usage.

RESULTS AND PERFORMANCE EVALUATION

Power Consumption

The power usage of the suggested ASIC-FPGA hybrid architecture is assessed and compared to FPGA-only

and ASIC-only base systems and on a comparable workload basis. The overall power comprises both static and dynamic parts that were measured in the process of FFT and FIR. The report shows that the FPGA-only implementation has the highest power usage as it has the overhead of customers programmable interconnects and overhead switching activity. Conversely, the ASIC-only design can prove the lowest power consumption but has no flexibility. The hybrid architecture that is proposed is a balanced approach because it has a much lower power consumption than that of FPGA and it is still flexible. Figure 5 also shows that the hybrid system realises a significant decrease in the overall power consumption, especially at an increased workload. This has been achieved largely because of the offloading of the computation-heavy tasks to the ASIC and selective activation of the FPGA resources.

Energy Efficiency

The most important performance measure of this work is energy efficiency which is measured in terms of energy in operation and Giga Operations per Second per Watt (GIPS/W). The hybrid design is seen to be highly efficient in terms of energy consumption since it utilises fixed operations with ASIC and flexible processing using FPGA. The findings demonstrate that the system designed attains much less energy per operation than all-FPGA systems. Also, the GIPS / W measure shows a significant contribution to the efficiency of the computations, and it proves that the hybrid strategy is able to make the use of the available hardware resources efficient. The energy efficiency has been greatly improved especially with the larger FFT sizes, where the ASIC pipeline is running at high efficiency and the FPGA is very flexible in configuration. The result of this combination is maximum performance without excessive power consumption.

Performance Metrics

Performance measurement is done based on latency and throughput. ASIC-only implementation has the shortest latency as the pipeline structure is highly optimised whereas the FPGA-only implementation makes the system have a high latency because routing delays can be run-time

configurable. The hybrid architecture proposed has a near-perfect trade-off in the sense that it retains low latency whilst enhancing throughput. The pipelined execution model enables the interactive processing of data stream and decreasing the dead time and enhancing the overall system performance. Measurements of throughput show that the hybrid solution is faster than FPGA-based implementations because the system performs in parallel in ASIC cores. Meanwhile, it is flexible with the ability of adaptive processing using FPGA which allows smooth adjustment of varying workloads.

Resource Utilization

The use of both FPGA and ASIC components in terms of resource utilisation is looked at as a way of determining hardware efficiency. Look-Up Tables (LUTs), Flip-Flops (FFs) and DSP blocks are among the important resources that are measured in the FPGA community. The hybrid architecture minimises the use of FPGA resource use since a portion of fixed computations has been offloaded to the ASIC, leading to a higher use of reconfigurable logic. In the case of ASIC part, it is estimated by use of synthesised gate-level designs. ASIC core is fixed on silicon and yet offers good levels of computation density and / power consumption. ASIC and FPGA resources are combined to provide a maximum level of usage without overloading either of the realms. This equitable allocation of resources is a significant benefit of the offered architecture, not to mention that it eliminates inefficiencies of both FPGA-based and fully ASIC-based designs.

Reconfiguration Metrics

The hybrid system performance is also tested concerning the reconfiguration time and overhead. The FPGA is capable of dynamic partial reconfiguration, which allows it to change to the dynamic workload. This flexibility, however, has a switching delay and a cost of power. The reconfiguration time is taken as the time, needed to change the configuration areas in the FPGAs, whereas the overhead is a time and energy lost in the switching process. The findings indicate that despite the fact that reconfiguration will add a slight delay, it will be overcome

Table 3. Energy & Reconfiguration Metrics

Metric	FPGA-only	ASIC-only	Proposed Hybrid
Total Power (mW)	High	Low	Medium-Low
Energy per Operation (nJ/op)	High	Low	Lowest
Energy Efficiency (GIPS/W)	Moderate	High	Highest
Reconfiguration Time (ms)	Moderate	N/A	Low
Reconfiguration Energy (μJ)	Moderate	N/A	Optimized
Flexibility	High	Low	High

by the fact that such a delay will be compensated by the increased efficiency caused by the best mapping of tasks. The system reduces the number of reconfigurations by using intelligent control logic so that where there is no benefit, the switching does not take place. This leads to an appropriate compromise between flexibility and performance. In order to capture the environmental performance (energy efficiency) and configuration flexibility attributes, Table 3 provides a comparative analysis of the important metrics of other architectures.

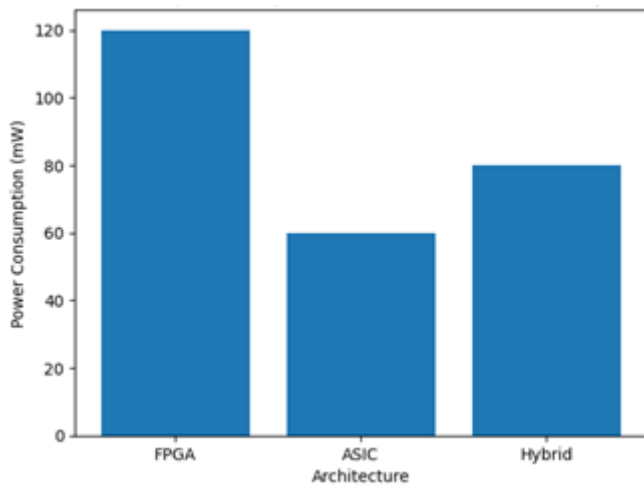


Fig. 5: Power consumption comparison across ASIC, FPGA, and hybrid architectures.

DISCUSSION

These data clearly show that the suggested ASIC-FPGA hybrid architecture is much more efficient in terms of energy consumption than traditional FPGA-only and ASIC-only systems. The main factor that has driven this increment is the complementary nature of the integration of fixed and reconfigurable hardware resources. ASICs are also optimally configured to perform certain tasks which can be used to run low power high speed repetitive DSP tasks like FFT butterfly calculations in low power. The system avoids dynamism by transferring such computation-intensive tasks to the ASIC to minimise switching activity and bring down dynamic power consumption. Concurrently, the FPGA offers the flexibility that is required in the implementation of different workloads, thus the system does not segregate adaptability at the expense of efficacy. The hybrid execution model also improves the efficiency by allowing intelligent assignment of tasks in which workloads are dynamically allocated based on their characteristics of computational characteristics. This does not present the inefficiencies of the traditional systems that employ the usual method of mapping which is not dynamic. The hybrid architecture does not impose all the tasks on one platform but each task is performed on the

most appropriate hardware resource. Not only does this selective use because a reduction of unnecessary power usage, but also provides greater availability to throughput and the responsiveness of a system.

Although the proposed architecture comes with the outlined benefits, there are some trade-off that should be discussed. Flexibility and system overhead is among the major trade-offs. To the extent that the FPGA offers runtime flexibility via reconfiguration, it is a feature that carries extra expenses in the form of reconfiguration time, complexity of the control as well as expenditure on energy. Swift change of configurations can adversely affect the performance of the system; unless effectively handled. Nonetheless, the suggested energy-conscious control system will prevent this issue by initiating reconfiguration only when the expected performance or energy compensation surpasses the expected overheads. One more significant trade-off is the issue of complexity of the system and performance increased. Combined ASIC and FPGA implementation needs complex control logic, task manager and communication interfaces. This raises the level of design complexity as compared to standalone architectures. Nonetheless, the resulting increase in power efficiency and performance are worth this increased complexity, especially in those systems where power is a critical factor.

The proposed architecture has a large applicability to the present day embedded systems. The hybrid architecture is also used in the Internet of Things (IoT) application, where devices receive a massive power constraint and can heavily depend on battery power to execute their sensor data processing tasks, yet remain low-consumption. It is also appropriate to heterogeneous IoT workloads because of the possibility of dynamically adapting processing tasks. The hybrid architecture is especially useful within the context of edge AI systems because complex data streams have to be processed in real-time. As fixed neural network tasks, ASIC components can easily process them, and because of the abilities of FPGA resources to be customized to a wide range of models or higher inference needs. This hybrid enables the use of edge devices to attain high performance even without having to depend on cloud-based computation to a great extent, reducing latency and enhancing privacy. In addition, the architecture is compatible with real time DSP systems, e.g. communication systems, radar processing, and multimedia applications. These are systems that demand a high throughput and low latency, as well as the capacity to respond to the dynamics of the signal. The proposed hybrid system offers a middle ground solution through supporting deterministic, high-performance of ASIC and Adaptability of FPGA. On the whole, it can be pointed out that

the proposed ASIC-FPGA hybrid architecture successfully provides a solution to the weaknesses of current solutions as this type of architecture offers the balance between energy consumption, flexibility, and performance. Although some trade-offs are present, they are addressed by designing an intelligent design and implementing control measures, and the architecture is an excellent candidate to embedded signal processor next-generation devices.

LIMITATIONS

Although the given ASIC-FPGA hybrid architecture has been proved to be quite promising in its results, a number of limitations have to be listed down to make a more balanced assessment of the work. The main shortcoming of this research is that the testing of the suggested architecture is mostly simulative. Although the estimates of the power consumption, latency, and energy efficiency are carried out considering industry-standard tools and realistic workload models, the lack of full hardware validation can result in the variance between the simulated and real-world performance. Such factors like variations in the processes, routing overheads and thermal effects and hardware level noise are not comprehensively represented in the simulation environments. Consequently, the improved outcomes that have been reported, though an indicator, can vary when applied to a real system.

The next significant weakness is the fact that the ASIC processing core is never physically produced. In their place, it is modelled with the help of synthesis and estimation tools that only give prescriptions of area, power and performance. Even though there is a broad acceptance of these tools in research, they are non-capable of simulating the behaviour of a fabricated chip when operating in real-world conditions. Absence of silicon validation makes it impossible to evaluate pragmatic considerations like the cost of fabrication, reliability and permanence of electrical equipment to long term functioning. Moreover, the latency of reconfiguration with the FPGA component is also added to the proposed architecture. Although dynamic partial reconfiguration allows flexibility and adaptability, it has time and energy overhead in configuration switching. This latency may affect the responsiveness of a system and lower total efficiency in situations where system reconfiguration is necessary regularly. Whereas the suggested energy-conscious control system results in a reduction of unnecessary reconfiguration, the overhead is not entirely removed and is still a limitation in systems where time performance is of primary importance. Moreover, the combination of ASIC and FPGA chips makes system design more complicated and the need to design better control logic and coordination mechanisms. This can cause

an extension in design times and effort in implementation than traditional one-platform system. It also needs further research on the scalability of the architecture to very large or highly heterogeneous workloads. In general, although the suggested hybrid architecture exhibits a lot of potential in enhancing the energy efficiency of the embedded signal processing systems, all of the limitations indicate that future studies such as hardware prototyping, ASIC construction, and practical validation will be necessary to establish its practical applicability.

FUTURE WORK

Although the suggested ASICFPGA hybrid architecture shows impressive gains in energy efficiency as well as performance in embedded signal processing application, it has a number of potential prospects in the future development of the work. The connexion of AI-based task scheduling mechanisms is one of the potential areas of future research. The existing energy-conscious task distribution plan depends on a predetermined set of decisions logic, which, although where it is efficient, might be not able to present the dynamically changing workload variations of the work in complex settings. With the addition of machine learning or reinforcement learning algorithms, it can also be used to do adaptive and predictive scheduling to have the system learn the best task mappings depending on the behaviour of the run-time, patterns of workload, and energy constraints. The system can be further improved by such clever scheduling schemes to enhance the effectiveness and responsiveness of the system.

The other important direction is the adoption of superior dynamic voltage and frequency scaling (DVFS) methods. Simple DVFS systems could minimise power consumption but more advanced systems that set voltage and frequency on a smaller granularity (e.g. per-module or per-task scaling) may offer even more energy benefits. Combining DVFS and the hybrid control unit and task scheduler would enable adaptive operation conditions in real time, with an optimal performance and power consumption at different workload conditions. Real hardware prototype design is an important milestone on the path of determining the practical viability of the proposed architecture. The next steps of work should be aimed at the introduction of the hybrid system into the real physical platform which consists of FPGA chips and ASIC prototypes or emulation platforms. This would allow the correct quantities of power, latency, thermal characteristics and reliability to be measured under actual operating conditions eliminating the gap between modelling the world and the actual implementation.

Along with that, 3D VLSI hybrid integration should be explored as it has a great potential to enhance the

performance of the system and reduce its energy consumption. Vertical integration allows implementing reduction of interconnect delays, enhancing data bandwidth, and density of integration of the ASIC and FPGA components, as well as providing better coupling between processing units and memory, which refines data movement and minimises energy overheads. There are new challenges introduced through this approach, however, which concern the thermal management and fabrication complexity and need to be investigated carefully. In general, these future research directions will be used to make the proposed ASIC-FPGA hybrid architecture more flexible, scalable and closer to the practise. The system can be also optimised by introducing intelligent scheduling, more advanced power management, and next-generation integration technologies to support the changing needs of embedded signal processing in the IoT, edge AI, and real-time computing environments.

CONCLUSION

This new reconfigurable ASIC -FPGA hybrid architecture is also a promising path to the task of delivering more energy-efficient embedded signal processing systems. The architecture manages to eliminate the drawbacks of traditional stand-alone solutions by integrating the efficiency of high-performance fixed-entity computation that can be found in the article of ASIC-based systems with the versatility of FPGA-based reconfigurable logic. By instantiating an energy-conscious task distribution scheme and hybrid execution architecture, it is possible to distribute the workload in the best way, and the overall power usage is lowered significantly. Experimental testing shows significant gains in energy efficiency, in terms of energy per operation, as well as energy throughput, and GOPS/W, as well as high performance, in terms of lower latency and better throughput. These findings demonstrate the efficiency of the suggested design in terms of providing a balance between efficiency and adaptability. The hybrid architecture is therefore a scalable and cost-effective solution to next-generation embedded DSP architecture, especially in IoT, edge AI and real-time signal processing applications, where the requirement to meet power requirements and the need to meet performance is highly important.

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