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RESEARCH ARTICLE

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A Low Noise Potential Divider Based Instrumentation Amplifier for Biomedical Retina Application

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Abstract

A potential divider-based instrumentation amplifier with a high CMRR and low noise is intended for use in biomedical applications. The goal of the suggested solution is to accurately remove the 10-bit DAC's high noise level. The 10-bit DAC has a power dissipation of 4.2µW and an open-loop gain of 52.65dB. Its sampling speed is 10MS/s, and its measured noise is 27.4920µv/√Hz. The suggested bio-potential instrumentation amplifier reduces the noise and power trade-off and boosts the output signal voltage by serving as a sensor interface to enhance electrical activity within the retina. The simulation results show a minimum of 133.0563nv/Hz at 1-50Hz and a maximum of 181nv/Hz with output noise; it is based on a 180nm CMOS process. With a power supply rejection ratio of 89.9dB, a slew rate of 9v/µs, and an amplifier power usage of 2.896µW at a Vdd of 1.8 v, it is far more suitable to stimulate the remaining retinal neurons.

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Introduction

The best electronic tool for analysing and boosting signals is an instrumentation amplifier (INA). Any transmitted signal is additive to several sounds, such as heat, shot, flicker, transit time, high-frequency component noises, and so forth, depending on the circuit architecture. In biological sensor systems, the transmission of an electrical signal instead of noise is crucial. An INA was created to increase signal strength by lowering the circuit layout's maximum noise levels. However, because of its exact common-mode rejection ratio (CMRR) and ability to remove disruptive high-frequency components, the proposed INA is used in retina implant applications. These discovery processes offer hope in biomedical applications to create practical technologies for human civilisation as technological scaling advances to better digital integration. Signal propagation starts with the image sensor and moves through the Analog to Digital Converter (ADC), Digital to Analog Converter (DAC), and retina portion in the creation of a Bionic Eye (retina implant). The proposed INA uses the digital integration technique to create a signal pathway to the retina implant through the DAC.[1] Electrodes in a brain simulator use an external driver device called a DAC to produce a charge-balanced biphasic current pulse to cerebral tissue.[2–3] The design of a standard 10-bit R-2R ladder DAC with linear resistors based on close/open switch functionality is covered in this study, along with the implementation of suggested INA characteristics.

10-bit R-2R Digital to Analog Converter

The DAC is an electrical instrument that converts a finite-state digital value into a physical quantity like current or voltage. Each bit functions as a switch in 10-bit DAC uses a R-2R type shown in Fig 1; if the bit value is high, the switch is connected to the inverting terminal of operational amplifiers (op-amp); if not, it is connected to ground.[4–6]

While the transistors in a DAC binary weighted resistor work as switches, the output voltage generated is determined by the specifications of the op-amp. On the other hand, weighted resistors are highly susceptible to noise. Consequently, the DAC with the specified INA needs to obtain design requirements for improved characteristic evaluation.

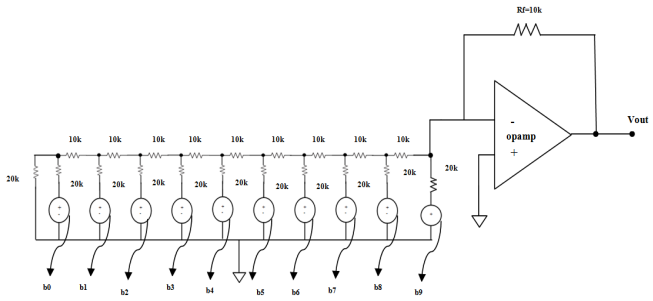

Fig. 1: Schematic of 10-bit R-2R ladder DAC.

Fig. 2(a) illustrates how the configuration, voltage source, transistors' W/L ratio, constituent quantities with preferred gain, along with enhanced slew rate, significantly impact the design of an op-amp. An output buffer stage, a voltage amplifier unit including biasing, and a differential input are often found in an op-amp3[7] M1, M2, M3, and M4 transistors are used for differential amplifiers, which are infamous for being current mirrors. Whereas M5, M6 transistors are used to carry high amplifier gain, and overall M5, M6, M7, M8 transistors are used for biasing, as shown in Fig. 2(b).[8, 9]

Every transistor (M1 to M8) operates in a region of saturation with the (W/L) ratio specified in the table. II in order to achieve the Table. I parametric values. Additionally, they guarantee that the simulated and theoretical findings for UGB, Gain, and Phase margin values are identical for an output response with a 180° phase shift, as shown in Fig. 3 (a) and 3(b), as given in the table. III.

The gain of the first stage is dictated by the transconductance of the M2, M4 transistors, the biasing current- I_{dc}, and the gain bandwidth-GB. On the other hand, the power consumption is computed using DC setup spectral analysis.

Table 1: Specifications for design

S.No.	Parameters	Value
1	Channel Length	180nm
2	Phase Margin	>60°
3	Open-loop gain	>40dB
4	Load Capacitance (CL)	1-10 pF
5	Maximum power dissipation	m-µW
6	Power supply	~1V
7	Unity Gain Bandwidth (UGB)	>5 MHz

Table 2: Transistors W/L values

S.No.	Transistors	W value (um)	Length (nm)
1	M1	12	180
2	M2	12	180
3	M3	2.3	180
4	M4	2.3	180
5	M5	3.8	180
6	M6	31	180
7	M7	40	180
8	M8	3.8	180

Table 3: Performance Evaluation

Considerations	Theoretical value	Practical value
Power supply(v)	1	1.8
Open loop gain (dB)	>40	56.25
Phase Margin (°)	>60	70.2151
Unity Gain Bandwidth (UGB)-MHz	>5	9.86
Load Capacitance	1-10 pF	10 pF

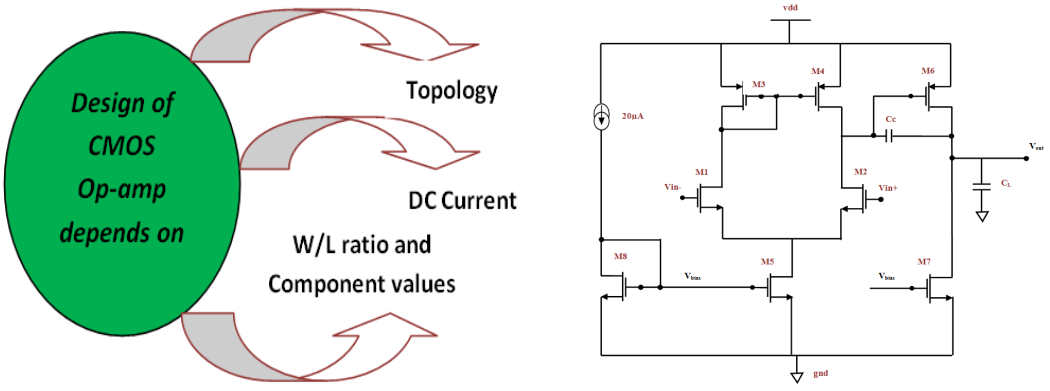

Fig. 2 (a and b): (a) Op-amp design elements. (b) Transistor level schematic.

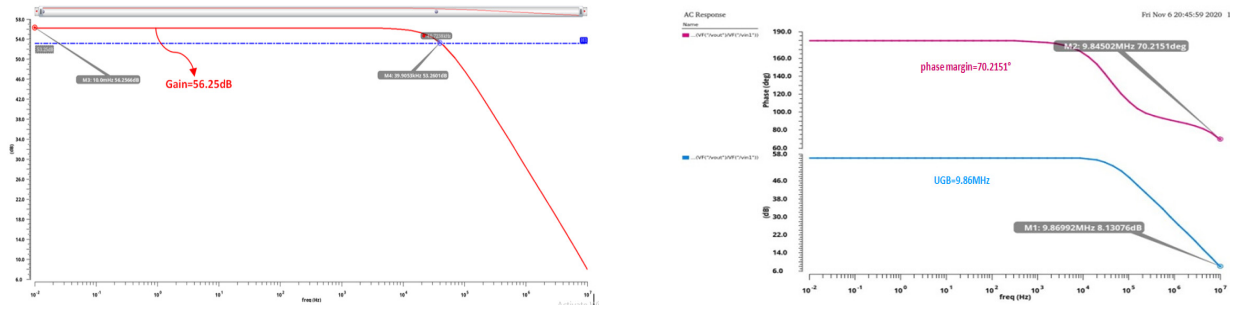

Fig. 3 (a and b): (a) Gain plot, (b). UGB plot & Phase Margin.

The resistor string seen in Fig. 4 is used to divide each bit via the DAC device's connection to the op-amp. For every resistance string, from MSB to LSB, the equivalent resistance is calculated. 'b0' equivalent resistor value = 20k//20k; 'b1' equivalent resistor value = (b0Req+10K)//20k; 'b2' equivalent resistor value = (b1Req+10K)//20k; 'b3' equivalent resistor value = (b2Req+10K)//20k; ... .; 'b9' equivalent resistor value = (b8Req+10K)//20k. However, because the resistive string is connected to the inverting terminal of the op-amp, Eq. 1 defines the design's gain, and Eq. 2 expresses the closed-loop gain in decibels.

$$Gain = \frac{V_{out}}{V_{in}} = \frac{-R_f}{R_{in}} \quad \text{Eq. 1.}$$

$$GainindB = 20\log\left(\frac{V_{out}}{V_{in}}\right) \quad \text{Eq. 2.}$$

The designed resistive feedback DAC is suitable for high-speed circuits with a sample rate of 10MS/s since it uses less power (6.24μW) than current-steering DACs. With a DNL/INL of 0.56/0.52, the LSB, the 10-bit DAC's final output is depicted in Fig. 5. By interconnecting the DAC with ADC, the SFDR (spurious free dynamic range) is measured, and it is stated as measuring the basic harmonic amplitude of the adjacent higher event through spectral analysis, it is of >60 dB.

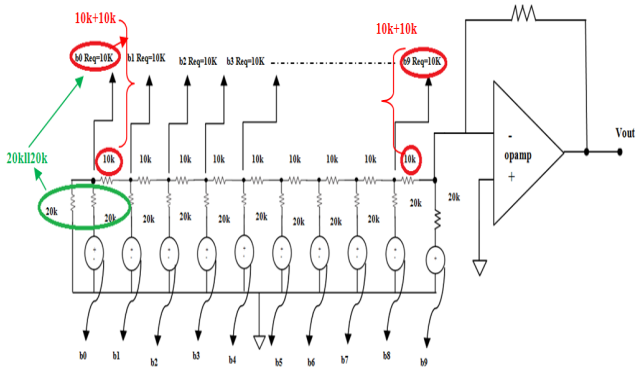

Fig. 4: DAC 10-bit Resistive network.

The 10-bit DAC's performance study is shown in Table IV, which shows that the intended sample rate of 10MS/s runs at 1.8v, reducing power consumption to 6.2μW. High-frequency noise components are removed more than in a conventional system due to the sample rate restriction [10–12], thereby reducing power consumption.

Nevertheless, analog signal of the DAC is affected by noises such as quantisation, device defect, and broadband and the offset variation, in particular, can cause the LSB value to become alert. Since the data signal is transferred in-line via an image sensor to the DAC, the output response in this study is probably an additive of different noise levels. The

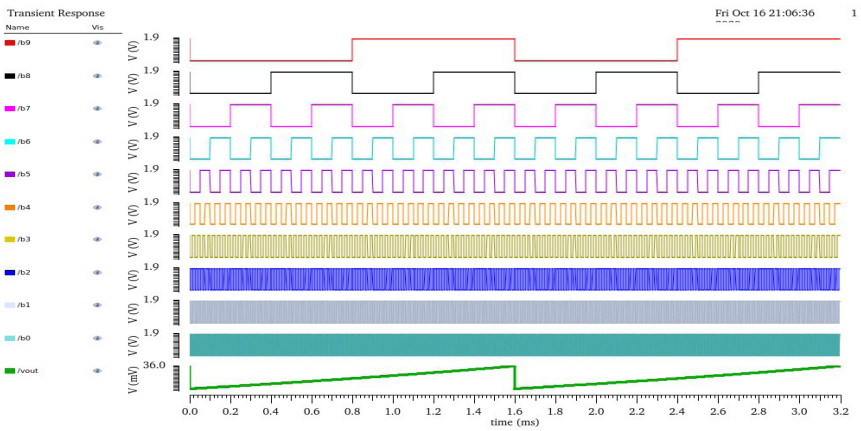

Fig. 5: DAC transient response.

Table 4: 10-bit DAC Performance Analysis.

Parameters	Ref [10]	Ref[11]	Ref [12]	This work
Supply voltage (v)	1.8	1.35	1.8	1.8
Technology (nm)	180	180	180	180
Resolution (bits)	10	12	10	10
Architecture	R-2R ladder	R-2R ladder	R-2R ladder	R-2R ladder
DNL/INL	0.178/0.496LSB	6.38/7.55LSB	0.7/0.75LSB	0.56/0.52LSB
Sample rate (S/s)	1G	20M	22M	10M
Power dissipation (W)	78.2m	1.7m	2.3m	6.3µ

generated output in the ADEL environment is subjected to noise analysis at the DAC stage; the measured value is 27.4920µv/√Hz, as shown in Fig. 6.

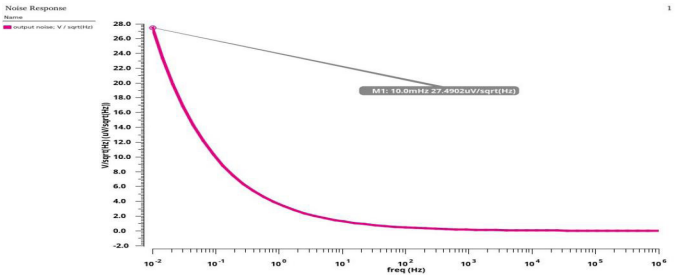

Fig. 6: 10-bit DAC noise plot.

DAC with Instrumentation Amplifier

By providing a high gain with a more precise and steady Common Mode Rejection Ratio (CMRR), a current-mode Instrumentation Amplifier (INA) improves optimisation by removing noise and DC offset [13–14]. A differential amplifier (A3), as shown in Fig. 7, is the most desirable due to its single gain resistance [15]. INA is internally made up of three op-amps that function as buffers (A1 & A2). Negative feedback results in voltage decreases across the gain resistor (Rg), which ultimately determines the closed-loop gain of the INA. Furthermore, a voltage reference (Vr) probably lowers the resistance mismatch impedance.

White noise and explosion noise further impair the DAC's performance. The measured output noise is 2.46µV/√Hz at 0-100Hz frequency, which reduces the DAC's typical noise. The amplification occurs between the output voltage of 0 to 1.7v. The output behaviour of the DAC with INA is shown in Fig. 8, where "Instout," the amplified result, is indicated.

The specifications are kept in the low frequency range, high CMRR of 100 dB to eliminate the common-mode signal, low output interference to the level of µv/√Hz, and sufficient signal amplitude (µv-mv) to have neuronal activity in the retina because the intended INA is intended to be integrated with the retina implantable design [16,20,21]. In order to aggregate the aforementioned requirements, the proposed INA is designed using a potential divider-based RC low pass filter, as shown in Fg.9(a).

Proposed Instrumentation Amplifier (INA)

The designed INA is made to be sustainable for low voltage applications and to function at a low frequency range with a high CMRR. An RC low pass filter removes the high-frequency components of the output signal, resulting in an output voltage of 994.05 mv. As shown in Fig. 9(b), a voltage divider used to attenuate the voltage

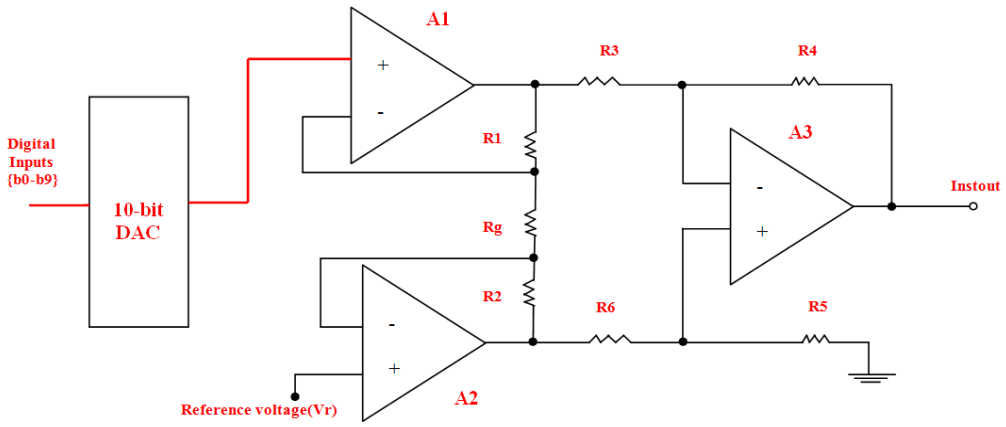

Fig.7. Integrated 10-bit DAC with INA

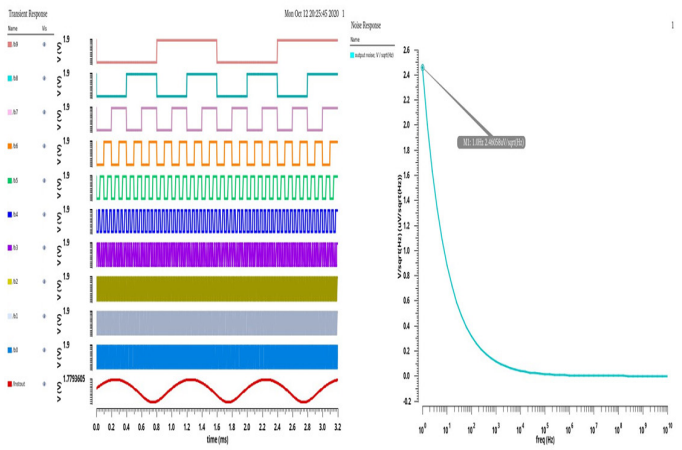

Fig. 8: Transient response and noise graph of DAC with INA

output from INA to the necessary level is described by Eq. 3. Its noise level is smaller than the typical DAC noise, with a maximum of 181 nV/√Hz at 0 Hz and a minimum of 133.0563 nV/√Hz at 50 Hz.

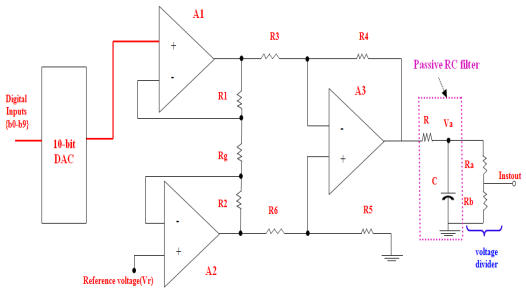

Fig.9 (a). Proposed INA design (i). Resistor values as R1=R2=22k, R3=R6=10k, R4=R5=47k, Rg=10k (ii). RC low pass filter R=1.5k, C=47nF (iii). Voltage divider of Ra=Rb=1k.

$$V_o = \frac{R_b}{R_a + R_b} V_a \qquad \text{Eq. (3).}$$

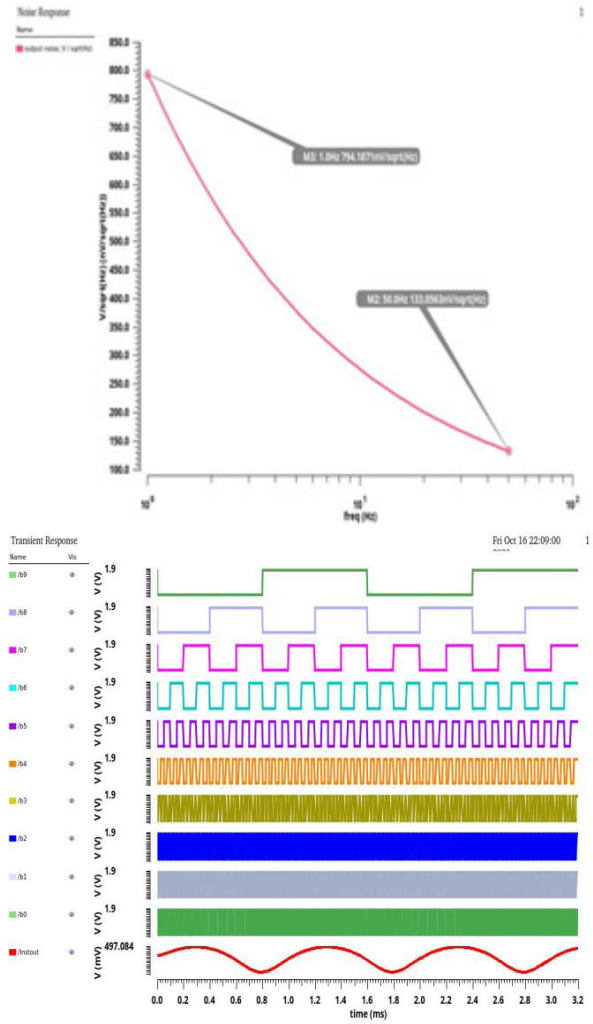

Fig.9(b). Proposed INA Noise response with output

Test-bench for the proposed INA's CMRR, PSRR, and slew rate

The test configuration for determining parametric parameters such as PSRR, CMRR, and slew rate is shown in Fig. 10(a, b, c). In terms of slew rate, the designed INA

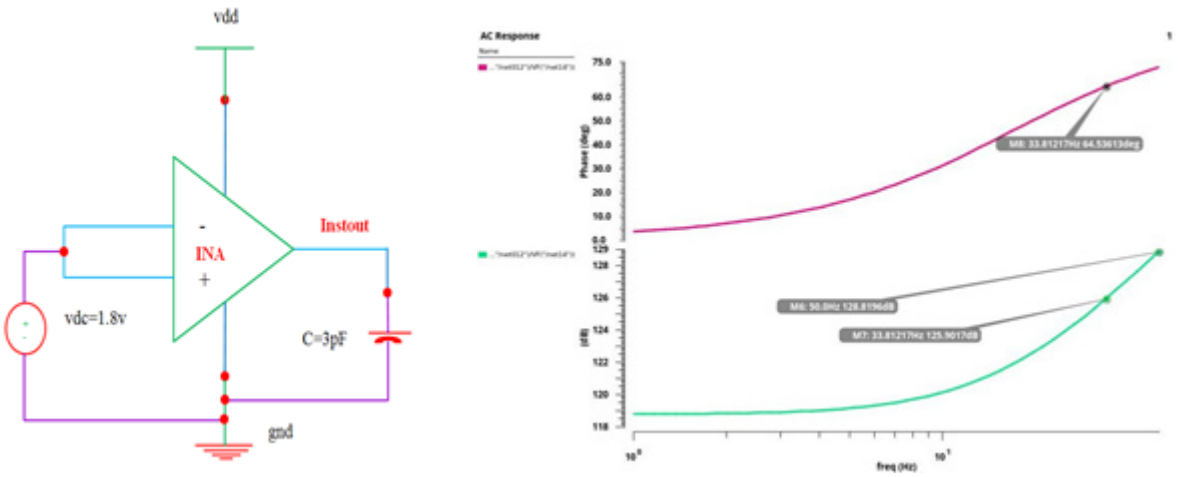

Fig.10(a): The proposed INA's CMRR test-bench.

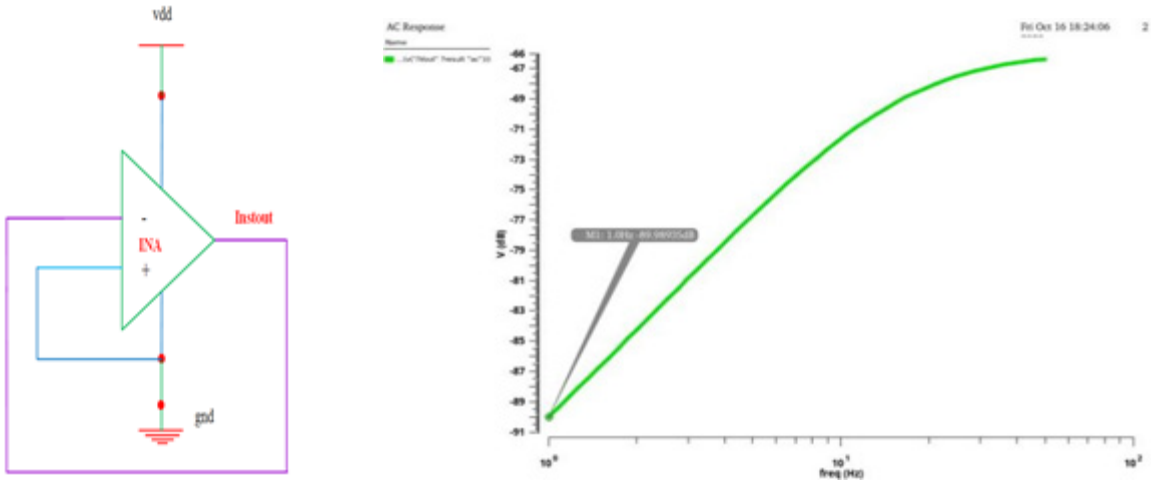

Fig.10(b): The proposed INA's PSRR test-bench.

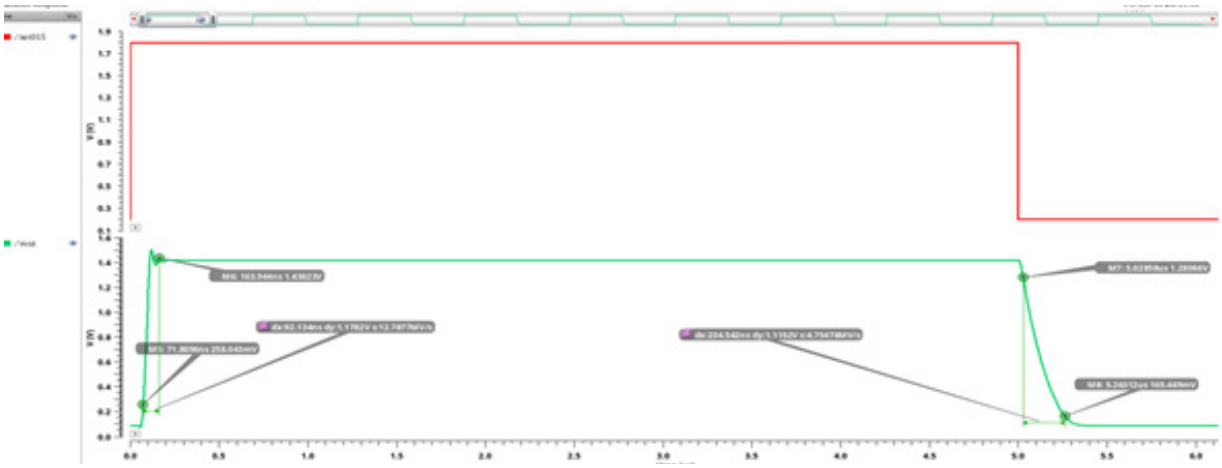

Fig.10(c): Slew rate.

Table 5: Summary table of Proposed INA

Parameters	Reference [17]	Reference [18]	Reference [19]	Proposed INA
Technology (nm)	180	180	180	180
Supply voltage (v)	3.3	1	1.8	1.8
Power Dissipation (W)	1m	1µ	4.07µ	2.86µ
Gain (dB)	80	59	39.75	85
Bandwidth (Hz)	10k	10k	0.3-4.4k	1-50
PSRR (dB)	-	-	-	89.92
CMRR (dB)	110	105	76	124.3
Slewrate(V/µs)	-	-	-	9

produces more satisfactory results. This indicates that the amplifier responds to a step voltage input significantly more instant of 9volt/sec, by instantly changing the output.

The designed INA can withstand circuit for power source variations up to 89.9 dB and offers significant CMRR with less power dissipation, according to the table. V.

Conclusion

The proposed INA is highly adaptable for biological applications, simulating the residual bio-potential neurons within the retina. The conventional DAC R-2R has a nominal voltage swing and consumes more noise, but at 10 MS/s sampling speed, it has a lower variance of 0.56 LSB step width. Accordingly, the simulation results

proved that the potential divisor INA outperforms the traditional INA with DAC in terms of rail-to-rail output swing for frequencies between 1 and 50 Hz with a CMRR of over 100 dB and condensed noise. Therefore, for low-frequency ranges, the proposedinstrumentation amplifier design can be utilised in biological applications.

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