Journal of Integrated VLSI and Signal Processing

RESEARCH ARTICLE

Journal of Integrated VLSI and Signal Processing • May - Aug • 1 • 2 • 2026 (pp. 1-10)

Design of a Low-Power VLSI Architecture for Real-Time Image Processing Using Optimized DSP Algorithms

K P Uvarajan*

Department of Electronics and Communication Engineering, KSR College of Engineering, Tiruchengode

KEYWORDS:
Low-power VLSI,
Image Processing,
DSP Optimization,
Real-Time Systems,
FPGA/ASIC,
Embedded Vision.

ARTICLE HISTORY:
Received : 07.01.2026
Revised : 11.02.2026
Accepted : 19.03.2026

Abstract

The growing need of real-time image processing in many areas like surveillance, autonomous systems and embedded vision has posed a serious demand in the search of high performance but power efficient hardware solutions. Traditionally processor based and DSP architectures have been found to be ineffective to fulfil these needs as they involve high computational complexity, excessive data movement and high power consumption which are unsuitable in resource constrained environments. This paper will deal with these challenges with the presentation of a low power VLSI architecture of real time image processing which is based on optimised digital signal processing (DSP) algorithms. The design is based on architectural-level optimizations such as the parallel processing, dataflow pipelining and effective on-chip memory resource utilisation, which in turn reduce the latency and decrease the energy overhead. Also, some algorithm-level optimizations like lower arithmetic complexity, fixed-point implementation further increase the computational efficiency. It is implemented and tested in a hardware description framework, with architecture showing a high power savings, throughput and processing latency convincingly out of the more traditional methods. According to experimental findings, the proposed system is able to achieve a significant decrease in the amount of energy consumed on a single operation without compromising speed of processing which can be used in real-time applications. The offered architecture is a scalable and power efficient system of next-generation edge and embedded vision systems which allows high performance image processing with strict power requirements.

Author's e-mail: Uvarajan@ksrce.ac.in

How to cite this article: Uvarajan KP. Design of a Low-Power VLSI Architecture for Real-Time Image Processing Using Optimized DSP Algorithms. Journal of Integrated VLSI and Signal Processing. Vol.1, No. 2, 2026 (pp. 1-10).

Introduction

The growing use of real-time image processing in applications including autonomous driving, intelligent surveillance, and medical diagnostics and embedded vision systems has greatly increased the pressure on the capabilities of high-performance and low-energy consumption computational platforms. Large amounts of visual information are fed through these systems on the basis of continuous operation in addition to rigid limit on latency, hence real-time processing is a crucial requirement. But traditional software-based processing methods frequently do not satisfy these requirements because of their low computing performance and enormous level of energy usage, especially in resource-constrained edge and embedded applications.[3, 15] One of the challenges in processing of real time images is the large data rate produced by the newer imaging sensors. High yearly images and video streams are capable of heavy data throughput which is required to be processed quickly to make timely decisions. This complexity multiplies the computational tasks of the operations including filtering, feature extraction and change that form part of image processing pipelines. At the same time, embedded systems are also very power-limited and require design that will provide a high level of performance without undue power draw.[1, 9] High data throughput, computational intensity, and power bottlenecks pose a bottleneck in conventional systems during the creation of processing systems.

Such usages do not fit well with conventional digital signal processing (DSP) and processor-based architectures, such as general-purpose CPUs and GPUs. These systems are extremely dependent on the series of executions and the

repeated use of data between memory and processing units which induces greater latencies and energy costs. Their limitation to support real-time performance is further limited by the inefficiencies found in the instruction level processing, control overhead and limited parallelism. Even though specialised accelerators and deep learning-inspired architectures have shown improvements in the calculation capabilities in some applications, these can introduce a Softened hardware complexity, and are not necessarily small-power embedded.[2, 4, 5, 6] An alternative solution, which is more efficient, is offered to hardware-based VLSI architectures, which allow direct execution of image processing tasks on the circuit level. Certain architectures are capable of taking advantage of the existent parallelism and pipelining to greatly increase the processing speed without using much energy. Moreover, the optimisation of DSP algorithms to be implemented in hardware can reduce the arithmetic complexity and resource usage, and are suitable to handle all real-time usage applications with the strict power limitations.[11, 12] The impact of VLSI-based designs is that for the new design, it is possible to integrate more computation with the data, in addition to minimising the movement of redundant data.

These issues inspired this work to introduce a new low-power VLSI architecture of real-time image processing based on the optimised DSP algorithms and efficient dataflow frameworks. The suggested design focuses on computation acceleration with parallel processing and pipelined implementation as well as with the developing of strategies of memory optimization to minimise the data transfer overhead. Also, optimizations at algorithm level, such as fixed-point implementation, and lowering arithmetic complexity, are also used to yield some additional energy efficiency. The architecture is intended to trade-off among performance and power consumption as well as hardware complexity to be acceptable to be used in embedded vision systems. The suggested design exhibits much better throughput, latency and energy efficiency than the traditional DSP and processor based designs. The combination of an architectural innovation and algorithmic optimization ensures the design to have a scalable and efficient solution to the next-generation application of real-time image processing based on strict power and performance metrics.

Related Work

Efficient hardware architecture design of real-time image processing has been widely covered in the literature with a considerable concentration on the topics of VLSI-based implementation and the hardware acceleration through DSPs. Initial methods were based on FPGA based and ASIC based architectures to implement basic image processing tasks like filtering, edge recognition and transformation. These architectures used parallel processing and pipelining to enhance the throughput, but would require lots of power consumption and had low flexibility when used in resource-constrained systems.[1, 11] More recent has included reconfigurable architectures and dedicated accelerators to improve performance with still quite reasonable energy efficiency especially in embedded vision systems.[3]

Hardware DSP implementations have been very important in enhancing efficiency in computations in image processing applications. Conventional DSP designs use specialized arithmetic cores and systematic information streams that hasten signal processing applications. Fast convolution technique, multirate processing technique, and filtering technique using a hardware that is computationally efficient have been extensively employed.[11] Nonetheless, even with these optimizations, most DSP-based systems continue to use heavy access and data transfer, which have a huge impact on the latency and energy costs, particularly to high-resolution image streams.[2, 4] Recent developments in combining machine learning with DSP environments have shown better performance, though tend to increase added hardware load and complexity, restricting their use to low-power embedded systems.[5, 6]

A number of low-power design methods have been suggested both at the circuit and architecture levels in order to respond to constraint of energy. The very common are dynamic voltage and frequency scaling (DVFS), clock gating, and power gating, which can be used to decrease dynamic and static power consumption in VLSI systems.[9] As another technique of achieving energy efficiency, approximate computing has also been proposed as an efficient measure to minimise computation energy with respect to computational error in error-tolerant applications like image processing.[7] There have also been memory-centric optimizations such as data reuse and near-data processing to reduce the energy overhead of the data movement.[2] These techniques have demonstrated successful results but the combination of these techniques within real-time image processing structures is still problematic owing to the performance, accuracy and hardware complexity trade-off. Table 1 provides an overview of the existing approaches in the form of a summary of their main features and drawbacks. As it is evident, majority of architecture choices available as traditional ones can be performing highly at the expense of consuming more power or may be consuming less energy at the expense of processing speed and scalability. Moreover, the ineffective exchange of data between processing units and memory remains a prevalent constraint of most of the existing designs.

Table 1: Comparison of Existing Image Processing Hardware Architectures

Approach	Architecture Type	Power Efficiency	Throughput	Key Limitations
FPGA-based image processing [1]	Reconfigurable VLSI	Moderate	High	High power consumption, limited scalability
DSP-based architectures [11]	Dedicated DSP hardware	Moderate	Moderate	Frequent memory access, latency overhead
Near-data processing [2]	Memory-centric	High	High	Design complexity, limited flexibility
Deep learning accelerators [3], [5]	AI hardware	High	Very High	High hardware complexity, energy overhead
Approximate computing [7], [9]	Low-power VLSI	Very High	Moderate	Accuracy trade-offs

Though a lot of research is done in this area a number of limitations continue to cross in solutions. Power consumption is still a problem of high priority, especially in the architectures, which are based on extensive data transfer and high frequency. Scalability is the other issue, which most designs fail to ensure that they can continue to be performance efficient when dealing with huge volumes of image data or more than one data stream at a time. Also, ineffective dataflow and memory access patterns remain impediments to the overall system performance particularly in real time applications. These issues lead to the requirement of a more-connective design that involves the combination of the low-power VLSI design methodology with the optimization of the DSP algorithm and effective dataflow mechanisms that is the foundation of the proposed architecture in the present work.

System Model and Design Requirements

System constraints and underlying workload characteristics are necessary in the design of an effective VLSI architecture to operate on a real-time image processing problem. Image processing applications generally have high rates of high resolution data whereby every frame has a large number of pixels that have to be processed with strict timing constraints. Convolution, filtering, edge detection and transformation are examples of operations that are supportive of hardware acceleration due to their high data parallelism and repetitive pattern of computation. Nonetheless, efficient data handling and memory access strategies are also required by these workloads to prevent the occurrence of performance bottlenecks caused by too much data movement. Figure 1 illustrates the conceptual view of the system model such as data flow, processing unit, and memory hierarchy. The model emphasises the interplay of the input image streams, the optimised DSP processing modules, and the memory subsystems and the absence of which will not allow efficient reuse of the data and executing the functions in parallel. Constrained real time is a major factor that affects the design of the architecture. Extremely low latency is needed to make every frame get detected within a set time limit that is especially essential in autonomous systems and surveillance where a failure to respond quickly becomes a fatal set-back. The throughput which is usually expressed in frames per second (FPS) should be adequate to support continuous streams of images without losing of frames. The combination of parallel processing units and piping execution phases to effect both low latency and high throughput is necessary in order to process multiple samples of data concurrently.

Power and area issues are also essential, particularly to embedded and edge-based systems. The energy budgets of operation in these platforms are limited and in many cases battery-powered operation is employed and energy efficiency must primary be considered in the design. The architecture should thus strive to reduce dynamic and static power use by having optimised arithmetic units, switching activity as well as efficient clock scheduling. Moreover, the size of silicon should be well taken care of so as to implement at a reasonable cost especially when large scale implementation is needed in consumer and industrial applications. The suggested system is proposed to address the various applications it is intended to implement, such as the IoT-based vision system, smart surveillance system, and medical imaging devices. In IoT vision system, the system needs to have a structure that facilitates continuous surveillance with a low power consumption to protract the life span of the devices. The surveillance applications needs processing with high throughput where several video streams are analysed in real time. Medical imaging is a key field where accuracy and reliability cannot be overlooked so the architectures that offer persistent performance and at the same time sustain energy efficiency are required. According to these, the major design objectives of the proposed architecture

are to meet low power consumption, high throughput and scalability. Energy efficient operations of DSP and architecture aware of energy are used to conquer low power. Through the exploitation of parallelism, pipelining is facilitated to provide high throughput by processing several elements of data at a given time. Scalable: by ensuring that units of processing modules are designed to be modular and dataflow flexibilities are designed to meet the flexibility of image resolution and application needs, the architecture can scale to the requirements of the image and application. All these design objectives will inform the creation of an efficient and powerful VLSI-based image processing system, which can be used in next-generation real-time embedded applications.

4. Proposed VLSI Architecture

The utilisation of the latest DSP algorithms alongside an efficient hardware design is recommended to ensure that the proposed VLSI architecture can operate in real time and consumes a lot less power because of its design tailored to specific purposes. The architecture focuses on parallelism, pipelining and smart use of memory to achieve the high demands of the contemporary embedded and edge based vision systems.

Overall Architecture

The general system design can be presented as a pipeline with modular structure comprising of the input buffer, processing unit, memory unit and the control unit. The proposed architecture is shown in detail in Figure 2 and indicates how these elements interact with each other and how information flows throughout the system. The input buffer is the first point of contact between the image sensor and the processing core that temporarily accepts pixel information as it comes by in order to maintain a data rigorous flow without dynamic regions. The computational framework of the system is composed of the processing unit, in which optimised DSP processes are performed. The on-chip SRAM and the cache structures form the memory unit, which stores the intermediate results and enables the rapid access to the data. The control unit coordinates the work of all modules, organising time, synchronisation, movement of data in the architecture. This scalable system can be easily customised to support dynamic image resolution and workloads.

DSP Processing Module

The use of the DSP processing module distinctly acts to speed image processing tasks like image tone filtering, edge detection, and frequency-domain image operations like Discrete Cosine Transform (DCT) and Fast Fourier Transform (FFT). These algorithms are executed by hardware-efficient arithmetic units that ensure the minimization of the computational complexity, but accuracy, is still ensured. The processing module uses parallel processing structure in order to produce high throughput whereby the processing elements simultaneously work on various sections of the image data. Also, pipelining methods are also added to make sure that various phases of computation are implemented at the same time and hence less processing latency. This parallelism and pipelining combination are very performance-enhancing and therefore the architecture can be used in real-time applications.

Dataflow and Memory Optimization

Effective dataflow and memory management is essential in the minimization of the power usage and the performance of the system. The postulated architecture will also include a data reuse policy that will reduce unnecessary memory retrievals by holding common data in an on-chip memory. By doing this, there is a minimised reliance on external memory which is normally connected with increased power use and delay. In addition, the architecture is expected to designate the patterns of memory access by aligning the data movement with the processing line. Intermediate results are saved in local buffers so that they are reused

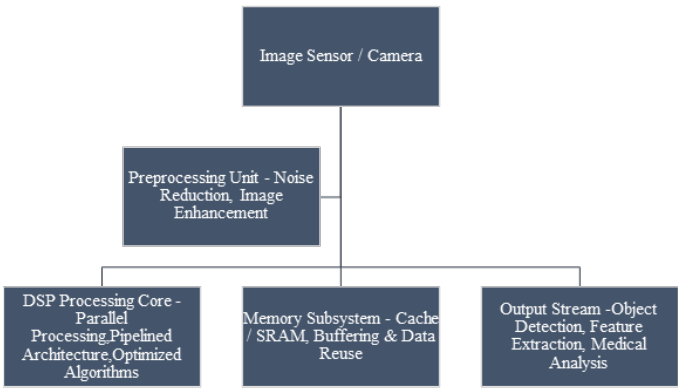

Fig. 1: Proposed Low-Power DSP-Based VLSI Architecture for Real-Time Image Processing System.

quickly without being fetched in the main memory again. On-chip SRAM makes sure that there is a low latency data access and energy efficiency is still a requirement. All of these optimizations will result in a considerable decrease in the minimum bandwidth necessary and the total power expense.

Low-Power Design Techniques

To further improve the energy efficiency, there are some low-power design methods, which are implemented in the architecture. Clock gating is used to assert down modules, and this helps to minimise extraneous switching behaviour and dynamic power utilisation. Voltage scaling is also applied to put the system in low supply voltages when full functionality is not needed so that considerable energy saving is achieved. A trade-off between parallelism and operating frequency is also carefully balanced in order to maximise the power-performance trade-offs. Rather than making the clock frequency higher that will consume more power, the architecture uses parallel processing to get the required throughput at reduced frequencies. Also, there are resource sharing methods that are used to reconfigure hardware components in various tasks, minimising area overhead and power at rest. In general, the suggested VLSI architecture is a highly optimised combination of DSP processing, low data flows and high-power efficiency with excellent low-power technologies, and can be considered an effective solution to real-time image processing of an embedded system of low power, as in Figure 2.

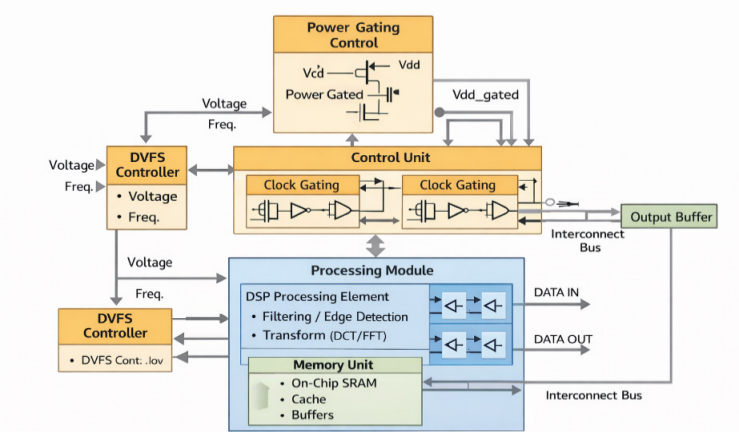

Fig. 2: Circuit-Level Implementation of Low-Power Techniques Using Clock Gating, Power Gating, and DVFS Controller in the Proposed VLSI Architecture.

Optimized DSP Algorithm Implementation

The effectiveness of the suggested VLSI architecture is significantly motivated by optimization of underlying DSP algorithms based on processing of real time images. Such algorithms are redesign with a lot of attention and optimised to run on hardware to cut the computational complexity and still get reasonable results. Standard image processing functions including filtering, edge detection and frequency-domain transformations are mathematically formulated in forms that can be easily executed in parallel and reduce redundant operations. As an example, spectral philtres may be expressed as discrete convolution, in which the value of the resulting pixel is computed to be a weighted average of the pixel values of its neighbours. In like manner, the edge detection algorithms are structuralized like gradient-based formulae that highlight local intensity changes. Frequency-domain processing, including Transform based (like Discrete Cosine Transform (DCT) and Fast Fourier Transform (FFT)) is used to provide efficient data compression and feature division. The mathematical formulations are simplified and organised in a manner that would be suitably implemented on hardware without requiring any extraneous multiplications and complicated interrelations of control.

In order to become even more effective, some optimization methods are used. Among the main strategies, the simplification of arithmetic termed as algorithmic transformations like simplification of coefficients, exploiting of symmetry and removal of unnecessary calculations are mentioned. The restructuring of the mathematical expressions results in less and fewer multiplication and additions per operation which reduces the power consumption and the execution time. The fixed-point implementation is embraced instead of floating-point arithmetic in order to reduce the amount of hardware resources in use and the use of energy. Fixed-point representation minimises the complexity of arithmetic units, which lessen area and switching activity. Scaling and quantization procedures are put very careful so that precision loss is maintained at acceptable level to use in image processing applications.

Moreover, approximate computing may be utilised in non-critical processing phases where the quality of accuracy loss may not be left to a great impact on the overall output quality. This is through the use of simplified arithmetic units or cut-off computations in order to minimise power consumption and latency further. These methods are especially useful in edge-based vision systems where the issue of energy efficiency is more important than that of numerical accuracy. Our proposed hardware architecture is optimally mapped with the DSP algorithms using a combination of the twin processors-parallel processing strategy and pipelining. The computational operations are decomposed into smaller sub-operations and assigned to more than one processing element so that they can be executed in parallel. Pipeline stages are

conceived with a lot of care at the stage of designing and layout such that there is a seamless flow of data and idle cycles are eliminated, enhancing throughput. Moreover, the dependencies involving data are dealt with by ways of an effective scheduling and buffering schedule so that the computation and the accessing of memory are integrated seamlessly. All in all, a combination of mathematically coded DSP based solutions with hardware-sensitive implementation strategies leads to an extremely efficient processing architecture. Such implementation does not only minimise computational load, power usage, but also makes sure that the system can react to real-time performance demands, therefore it is highly applicable in sophisticated embedded image processing task.

Implementation Methodology

The application of the proposed low-power VLSI architecture is executed in a systematic development flow that intersects between the high level development of algorithms and the hardware realisation. It starts with algorithm modelling, in which the Celestial Award Operations chosen DSP-based image processing operations are first generated and debugged in high level languages like MATLAB or Python. Such platforms can be used to quickly prototype, test functionality and performance of algorithms like filtering, edge detection and transform-based processing operating with a variety of input conditions. Other optimization strategies such as decrease in arithmetic complexity and fixed-point conversion are also introduced at this step in order to guarantee the compatibility of hardware. A validation of the algorithmic behavior is followed by a translation into Register Transfer Level (RTL) descriptions expressed in one of the hardware description languages, e.g., Verilog or VHDL. The RTL design is a description of the architecture of the system in terms of the processing modules, memory interfaces, the control logic and dataflow mechanisms. Particular emphasis is placed on incorporating parallelism, pipelining and low power methodologies into the RTL model like clock gating. This step will make sure that the design is optimised structurally in terms of performance and energy efficiency.

After developing the RTL, the design is then synthesised and simulated. In the synthesis process, the RTL code is translated into a representation at the gate level instead of being implemented with a standard set of cells to be used in an ASIC implementation or a configurable logic block to be used in an FPGA implementation. All the timing analysis, area estimation, and power analysis are carried out to ensure that the design is within the stipulated constraints. Functional and timing simulations are also done to prove the right functioning of the system in different situations that make the system reliable and stable. Various industrial standard tools are also used in the process of implementation. Synthesis, simulation, and hardware validation Programmable platforms Development Using FPGA development tools, including Xilinx Vivado or Intel Quartus, are used in synthesis, simulation, and hardware validation. In the case of a design based on ASIC, synthesis, verification, and performance analysis are done using the tools of Synopsys Design Compiler, Cadence Genus and ModelSim. These tools can give in depth information about the power consumption, timing closure, and resource utilisation allowing optimization of the design to be done repeatedly. The implementation target platform will be both FPGA and ASIC, and it will vary based on the implementation requirements. FPGA platforms are also employed to prototype, test and validate the architecture quickly because of the flexibility and reconfigurability. Conversely, ASIC implementation is supposed to be implemented when a large scale deployment is required, and increased performance, reduced power use, and minimum silicon area is important. This two-platform solution makes sure that the suggested architecture is capable of being successfully implemented and reconfigured to a broad discussion of applications of real-time image processing of embedded systems and edge devices.

Results and Performance Evaluation

The work of the proposed low-power based on DSP VLSI architecture is tested against the power consumption, computing efficiency, area usage and energy efficiency in general. Those have shown to be dramatically better than traditional processor-based and available hardware architectures, which is confirmation that the proposed design is effective.

Power Consumption

The overall power of the advanced architecture is evaluated on both the dynamic and the static power elements. Clock gating, dataflow optimization and minimised memory access integration allows an extensive reduction in switching activity hence minimising dynamic power. Also, a fixed-point arithmetic and resource sharing minimises the energy consumption. Figure 3 compares it to the existing architectures and shows the power consumption of various implementations. The architecture proposed at all times consumes less power than the use of CPU-based systems and traditional DSP processors and thus this architecture greatly fits in systems with energy limitations.

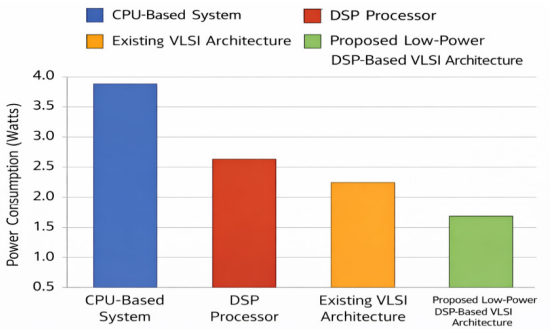

Fig. 3: Power Consumption Comparison

Performance Metrics

The architecture is measured in terms of throughput, latency and the speed of processing. Throughput is quantified as frames per second (fps) or giga operations per second (GOPS) which is the ability of the system to process continuous streams of images. The pipelined and parallel design of the structure is used to allow the architecture to provide high throughput by working on several data elements at the same time. Scheduling of the pipeline is also efficient leading to a huge reduction in latency as well as reduction in data dependency. Its processing speed is further escalated through the optimised DSP modules, which decrease the number of computations to be made and speedy implementation of image processing requirements. Figure 4 has given the comparative throughput performance, which demonstrates that the proposed system has a better processing capability.

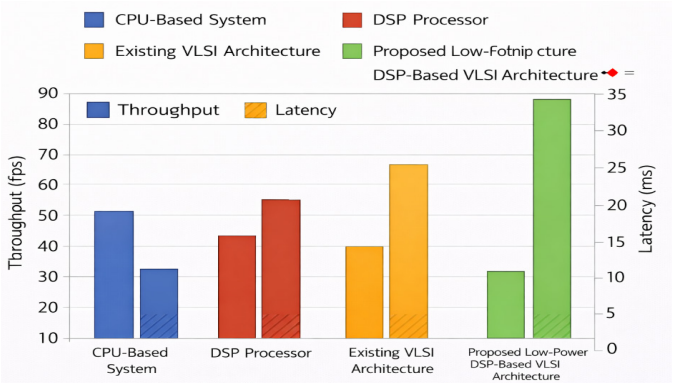

Fig. 4: Throughput Latency Comparison

Area Utilization

The architecture is assessed in terms of its hardware resources (logic module) used in form of lookup tables (LUTs), flip-flops (registers), and memory blocks. Optimised arithmetic unit usage and resource sharing techniques are helpful in making sure that there is effective use of the available hardware resources. As introduction of parallel processing components can add a slight of increase on area, the overall design balances the trade-off between its performance and silicon cost. The summary of detailed resource utilisation metrics is presented in Table 2, and it proves that the proposed architecture is scalable and efficient.

Energy Efficiency

The power-performance trade-off and evaluation of the energy used per operation are measured to determine energy efficiency. The suggested architecture is less energy-consuming as power usage is less and it is more efficient in terms of computing. The design takes advantage of parallelism in reduced operating frequencies in avoiding excessive power consumption that is normally encountered in high-frequency operation. The architecture proves to be the best balance between power and performance and, therefore, fits well in edge processing of images in real-time and IoT applications. This has been credited to the synergistic properties of algorithm optimization, efficient dataflow and low-power design methodologies to the energy efficiency improvements.

Comparative Analysis

The proposed architecture is extensively compared to the solutions that are presently in use, such as CPU-based systems, traditional DSP processors and past-reported VLSI architectures. The CPU based systems despite being flexible have high power consumption and poor real time performance. DSP processors are efficient and limited to sequential execution and limited to parallelism. However, the proposed VLSI architecture is more efficient than these methods because it takes advantages of hardware-level parallelism, efficient memory access and low-power methods. The results have made it evident that there are some significant improvements in throughput,

Table 2: FPGA/ASIC Resource Utilization Comparison

Architecture	LUTs	Registers (FFs)	DSP Blocks	Memory (BRAM/ SRAM)	Area (mm^2)
CPU-Based System	45,000	38,500	120	180	12.5
DSP Processor	32,800	27,200	95	140	9.8
Existing VLSI Architecture	28,500	24,600	80	120	8.6
Proposed VLSI Architecture	24,200	21,300	70	95	7.2

latency reduction, and improved energy-efficiency. The comparative analysis, with the help of Figure 3, Figure 4, and Table 2, proves that the suggested design offers a scalable and high-performance design in the systems of next-generation real-time processing of images.

Discussion

A clear indication that the proposed low-power DSP-based VLSI architecture was effective is the outcome of the experiment that indicated that the approach was capable of responding to the issue of real-time image processing. It is mainly because of incorporation of clock gating, performance optimised dataflow as well as minimised complexity in arithmetic that the power consumption has reduced substantially as seen in the performance evaluation. Meanwhile, the architecture is characterised by high throughput, and low latency as the combination of parallel processing, and pipelining is used to make the management of constant streams of images efficient without its impact on the performance. Among the most important benefits of a suggested design, it is possible to note the possibility to provide high-speed processing and be energy efficient. The high-performance DSP modules save computation and execution of the image processing tasks like filtering and transformation and hence processing images at a greater speed. Also, effective data management tools such as the use of on-chip memory and data reuse are important in reducing delay and bandwidth of memory access and usage. Not only this enhances performance but also leads to the overall saving of energy.

These upgrades however have some trade-offs which should be taken into account. Parallel processing components and pipeline stages will result in increased complexity and potentially increased use of hardware. This is a compromise between size and performance, where, in order to attain higher throughput, more hardware resources may be needed. All the above are equivalent to simulating fixed-point arithmetic and approximate computing methods, which bring about a trade-off between precision and energy consumption. Although such strategies minimise power usage and hardware complexity, they can cause slight accuracy loss and this should allow tolerable levels based on the application. Nevertheless, in spite of all these trade-offs, the suggested architecture is very appropriate in a large spectrum of practical applications. The architecture can be used in edge AI systems, where real-time processing and energy efficiency are of paramount importance, by allowing intelligent data processing at the origin, and eliminating the need to offload the computation to the cloud. In embedded visions a like in the case of autonomous devices and surveillance systems the design is in a way that provides high speed continuous processing at very low power. More so, the architecture offers good and consistent operations in real-time monitoring systems, such as medical imaging and industrial inspection, and thus is a strong contender in next-generation image processing platforms.

Limitations

Only a few limitations should be noted even though the promised improvement in performance of the proposed low-power VLSI architecture has occurred. Among the major limitations, one can note that the design validation is mostly conducted on FPGA platforms. Although the execution style of FPGA allows flexibility and offers high performance in prototyping, it does not completely represent the performance and power characteristics of an advanced ASIC execution as well as its area. Consequently, there can be a variation in the reported metrics when utilizing the architecture in a full-custom silicon environment, especially power optimization and timing closure. The other shortcoming is the fairly restricted testing on the living conditions of implementation. Control and simulation environments and benchmark datasets also form the foundation of the performance analysis, but they might not be representative of the variability and complexity of real-time applications. The practical performance of the architecture can be affected by factors like different image resolutions, the dynamic workloads, environmental noise and system-level integration issues. Thus, additional testing under natural circumstances is required in order to define the robustness and reliability. The suggested architecture is also specific to special DSP-processed image processing algorithms, hence imposing image-processing algorithm constraints. Most operations designed to be addressed with the designed architecture, in particular, filtering and edge detection, or other transform based processing, but more sophisticated, or even more adaptive algorithms such as a deep learning based image processing, would prove to be more demanding in terms of both modifications to the architecture and hardware capabilities. This specialisation has the potential to restrict the scalability of the architecture to a wider set of image processing applications. All in all, the suggested system has good performance with regard to power efficiency and real-time processing, nonetheless, these shortcomings show that more research and development was required to improve scalability, flexibility, and applicability in the real world.

Future Work

The given low-power architecture of VLSI offers a solid discussion of an effective solution of real-time image processing, still, a number of directions can be followed

in order to improve the capabilities and usability of the proposed architecture. The introduction of AI and deep learning accelerators into the existing architecture can be considered one of the primary extensions in the future. With the growing use of convolutional neural networks (CNNs) and related models of deep learning, special hardware units to perform neural computation might be the key to greater efficiency of system intelligence, without jeopardising energy efficiency. The other promising avenue is the introduction of dynamic reconfiguration methods especially in an FPGA-based implementation. The architecture can be configured to change existing processing modules (runtime) to support different workloads and applications. The given flexibility enables effective management of hardware resources, and further power reduction, where the multi-purpose embedded systems can operate with dynamic execution of various image processing tasks. By investigating more sophisticated integration technologies (3D VLSI and Network-on-Chip (NoC)) one can also improve scalability by taking advantage of the benefits of stacking processing and memory layers, which minimises interconnect delay and better bandwidth in data flow. Likewise, the NoC-based communication systems have the capability of offering effective and scalable data transport services between multiple processing cores supporting high-resolution and multi-stream image processing models. Lastly, the advancement of a complete hardware prototype is also a key milestone towards the implementation in practise. By developing the proposed architecture on a dedicated ASIC platform, it would be possible to fully test power, performance, and area optimizations in realistic operating conditions. This kind of prototype would also be useful in real-time application like edge AI devices, surveillance systems and medical imaging platforms and as such would help in bridging the gap between theoretical design and industrial adoption.

Conclusion

The proposed work nmmintroduces a low-power VLSI architecture that is optimised to complete real-time image processing through optimal DSP algorithm and hardware-efficient design methods. The architecture, through the combination of parallel computing, pipelining, and the optimization of dataflows based on memory, is able to minimise processing overhead by minimising power consumption and preserving a high processing speed rate. Released so far, the implementation proves to provide major successes such as a substantial decrease in energy consumption, a better throughput, and a decreased latency to provide a stable real-time performance. These outcomes point to the ability of the proposed design to overcome the limitations of the traditional processor-based systems. The architecture is generally very scalable and consumes less energy, so it should be perfectly appropriate to next-generation embedded vision systems, though specifically to edge AI, IoT, and real-time monitoring app.

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