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Design and Implementation of an Ultra-Low-Power VLSI Architecture for Energy-Constrained IoT Communication Systems

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ABSTRACT

The Internet of Things (IoT) is rapidly growing in number of devices and this has escalated the requirement of energy efficient communication, since most of the nodes have stringent power and battery limitations. Traditional VLSI designs are typically not able to balance between performance and ultra-low-power considerations, and are therefore not applicable in low-energy applications. This paper outlines the design and implementation of a VLSI architecture of extremely low power, optimized to IoT communication systems. The suggested architecture incorporates power-sensitive design approaches, such as clock gating, optimized data-paths and minimized switching power to considerably reduce both dynamic and leakage power. The design is actually taken and tested with standard CMOS technology and its performance is tested with different operating conditions. Experimental observations show significant power consumption is reduced when average power consumption is held constant and competitive throughput and latency is preserved. Notably, the architecture experiences low energy per bit, which makes it very suitable to continuous and battery-operated IoT applications. The proposed system demonstrates considerable improvement in overall energy efficiency over the current methods, and has power-performance trade-off improvements that can be measured. The findings affirm that the given VLSI architecture could efficiently combat critical energy considerations in IoT communications systems. The work adds a scale and energy-efficient solution that increases the life of any device and facilitates the sustainable implementation of the next-generation IoT networks.

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1. INTRODUCTION

With the swift increase in the number of Internet of Things (IoT) devices, there has emerged a high need to employ energy-efficient hardware, especially those related to communication, in its nature. IoT systems will frequently be used in energy-constrained deployments, where devices use battery resources or use limited energy sources to generate power, in which power consumption is a major design consideration. Recent research has revealed that the low-power sensing and monitoring systems are crucial in the working of the IoT, including structural health monitoring systems and embedded sensing systems [1]. Ultra-low-power circuit designs such as voltage and current reference circuits have demonstrated encouraging energy consumption levels down to pico-watt and nano-watt levels of energy [2], [3], [8], [13].

The importance of ultra-low-power communication architectures lies in the fact that communication subsystems of the IoT nodes take up most of the overall energy consumption. A variety of tools, including: adiabatic logic, charge recycling, operation of VLSI systems at low voltages, and so on, have been suggested to minimize dynamic and leakage power in VLSI systems [4], [6], [7]. Also, optimization of memory and analog circuits such as SRAM charge recycling, and low-power OTA designs can help to achieve better efficiency at the system level [10], [11]. The new applications like edge-based intelligent processing highlight even more the necessity to have energy-efficient hardware to meet the requirements of the real-time constraint [5].

In spite of these developments, current VLSI architectures are usually used to treat elements of a circuit but not a coherent design that takes the form of communication. Most solutions experience trade-offs between power, performance and area, which constrain their use in scalable IoT systems. Moreover, other important communication metrics like energy per bit have not been studied thoroughly as they directly influence system lifetime and efficiency.

Driven by these problems, this paper suggests an ultra-low-power VLSI design that is best suited to internet of things communication systems that are energy-constrained. The architecture incorporates both circuit and architectural power optimization strategies to realize substantial amounts of energy savings with no compromised communication performance.

The primary deliverables of this project are the creation of an energy-efficient design of an IoT communication system using a new ultra-low-power VLSI design. The proposed design is effectively modified to meet the strict energy limitation of IoT node by incorporating efficient power reduction strategy to combine clock gating, reduction in switching activity and low voltage operation. All these approaches help lower dynamic and leakage power resulting in a substantial increase in total energy efficiency. Specifically, the architecture has significant gains in important metrics like power consumption and energy per bit which is important in increasing the device lifetime in battery-operated conditions. In addition, an in-depth analysis is conducted to prove the efficiency of the suggested design, as it shows a better power-performance trade-offs in comparison with current designs. This renders the architecture a scalable and viable solution, next generation energy-constrained IoT communication applications.

2. Related Work

The current progress in the Low-power VLSI design has had a considerable impact on the design of energy-saving IoT systems. Various circuit-level designs have been suggested to overcome extreme energy requirements in IoT devices. To illustrate, IoT-based sensors focus on low-power usage to enable extended use in low-resource settings [1]. Besides that, voltage and current reference circuits that are designed with very low power, in the subthreshold and near-threshold regime, have also been demonstrated [2], [3], [8], [9], [12], [13], and with power consumption in the pico-watt and nano-watt scale.

A number of design methodologies have aimed at minimizing the power consumption through methods like adiabatic logic, charge recovery and minimizing switching activities [4], [6], [7]. These methods can be used to work effectively in minimizing dynamic power dissipation and enhancing energy efficiency on a circuit basis. Additionally, memory and analog circuit optimization, such as recycling of the charge stored in the SRAM and low power operation transconductance amplifiers (OTA) lead to higher system efficiency in total [10], [11]. Simultaneously, low power hardware acceleration methods to support edge-based IoT applications have been discussed to address the demands of real-time processing and reduce energy usage [5].

Most current literature however focuses on the individual components of a circuit, but not a complete VLSI-level architecture that would be specific to communication systems. Most designs can attain lower power consumption, but tend to reduce the performance measures, such as throughput and latency. Besides, despite being often reported, energy-saving metrics, like energy per bit and multi-metric measures such as energy-delay product (EDP) are not fully optimized and studied.

Thus, there is a gap in the optimization of energy per bit and overall efficiency measures in the literature, especially in integrated ultra-low-power VLSI platforms to support energy-limited IoT communication platforms.

3. Proposed VLSI Architecture

The suggested ultra-low-power VLSI architecture will aim at overcoming the strict constraints of IoT communication systems energy by incorporating energy-aware approaches at both architectural and circuit-levels. The entire system consists of three big modules, namely, the communication unit, the processing unit, and specific power optimization blocks. These modules have been well interlinked to make sure there is minimal energy requirement and to have a good data transmission and processing.

The communication unit at the system level is in charge of transmitting and receiving data and it integrates the use of energy efficient methods of encoding and decoding and minimizes switching activities. The processing unit offers simple data processing and control tasks, optimized to have low computational overhead. To further optimize power efficiency, blocks of power optimization are incorporated in the entire architecture, which allows controlling dynamic power consumption depending on the conditions of the workload.

The architecture uses some of the major low power design methods. Clock gating is also employed in order to turn off idle modules, which saves on unnecessary switching power. Moreover, power gating is used to reduce leakage power when in idle state. Voltage scaling is also implemented in the design enabling it to operate at lower supply voltages, greatly reduce dynamic power consumption. In the case of ultra-low-power operation, it is also possible to design components to operate in the subthreshold regime,

which can further decrease the energy usage without compromising the performance of the components.

A low power clock gating circuit is implemented to achieve such techniques and implemented into the architecture as depicted in Fig. 1 and this has the advantage of reducing dynamic power, since it regulates the clock distribution according to the activity.

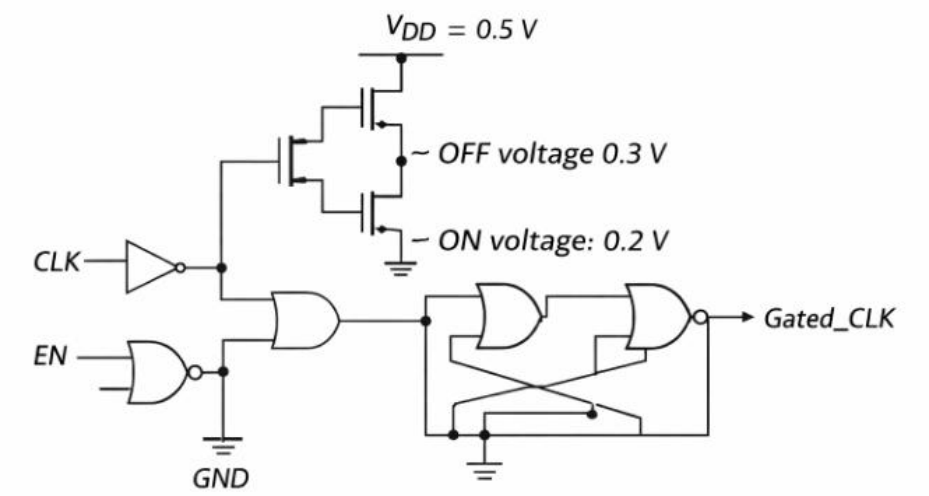

Fig. 1. Proposed ultra-low-power CMOS clock gating circuit with voltage scaling and switching control.

Moreover, to enable energy active data transmission, an optimized communication circuit is adopted as shown in Fig. 2, lower switching activity and less complex logic are designed to reduce energy per bit.

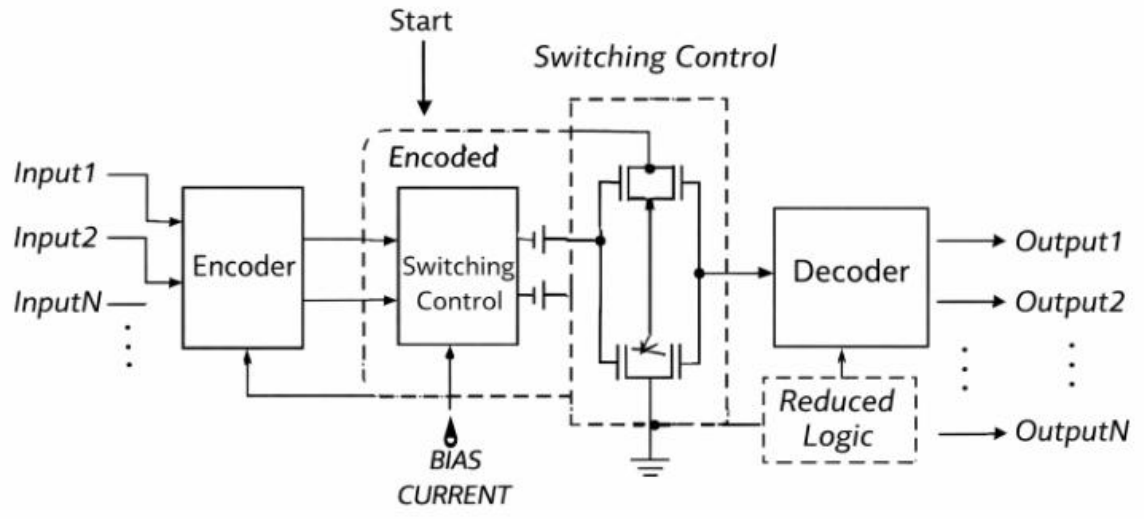

Fig. 2. Proposed ultra-low-power communication circuit with encoder–decoder architecture and switching control for energy-efficient IoT transmission.

All of these circuit-level and architectural optimizations allow the proposed system to make significant power savings and become much more energy-efficient and easily applicable to energy-limited IoT communication services.

4. Power Optimization Methodology

To support the practical use of the IoT in terms of energy-limited communication systems, the proposed VLSI architecture includes an extensive power optimization approach to reach the ultra-low-power operation. The design technique aims at reducing dynamic power, as well as leakage power, by both circuit and architecture level design.

The reduction in the dynamic power is attained by limiting switching activity and capacitive loading of the circuit. Clock gating, as explained in Section 5, can be used to turn off idle modules and hence, minimise clock transitions. Moreover data-path design is also optimized as well as the logic transitions are minimum which also helps in decreasing switching power.

Dynamism of the power consumption of the system can be represented as:

$$P_{dynamic} = \alpha C_L V_{DD}^2 f$$

where α is the switching activity factor, C_L is the load capacitance, V_{DD} is the supply voltage, and f is the operating frequency.

Leakage power, noteworthy at the deep-submicron level, is reduced by power gating and subthreshold operation methods. Leakage currents are avoided by selectively closing the idle circuit blocks and low supply voltages in operation. It can be approximated that the leakage power is:

$$P_{leakage} = I_{leak} . V_{DD}$$

To evaluate communication efficiency, the energy per bit metric is used, which is defined as:

$$E_{bit} = \frac{P_{total}}{R}$$

where P_{total} is the total power consumption and R is the data rate (throughput). This metric is critical for IoT systems, as it directly reflects the energy cost of transmitting a single bit of information.

The general power optimization procedure, also incorporating the switching reduction, scaling voltage and leakage control is depicted in Fig. 3 and represents the logical sequence of the techniques used in the proposed design.

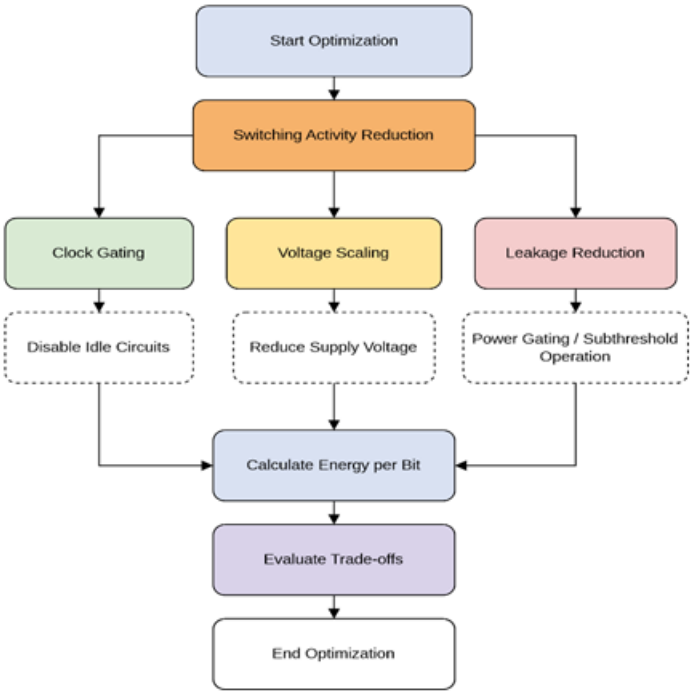

Fig. 3. Power optimization flow for ultra-low-power VLSI design.

One of the design factors that will be taken into consideration in the proposed architecture is a power versus performance trade-off. Although aggressive voltage scaling and subthreshold operation can greatly decrease power usage, it can also add more delay and throughput. Thus, it was carefully designed to balance these factors to attain optimum performance and still attain ultra-low energy consumption. This trade-off makes the architecture still be able to support real-time IoT communication applications without damaging the energy efficiency.

5. Implementation Details

The proposed ultra-low-power VLSI architecture uses a standard CMOS technology node to implement in the energy-constrained IoT communication applications. The design is modelled and tested both at the circuit and system level to guarantee proper assessment of power and performance measures. To validate hardware, the architecture may be instantiated on FPGA platforms, and extended to ASIC realization to achieve optimized energy efficiency.

Electronic design automation (EDA) tools that are industry standard are used in the design process. Simulation of circuit-level is conducted with SPICE based tools to test power consumption and switching attributes, synthesis and timing analysis is conducted with HDL based design tools. These tools can be used to estimate dynamic and leakage power and prove the functional correctness.

The operating conditions of the proposed system are carefully chosen to obtain ultra-low-power operation.

The design delivers smaller supply voltage (e.g., 0.5 V) to reduce the dynamic power consumption, but continues to work reliably. Operating frequency is operating within a relatively middle band (e.g., 100 kHz-some MHz) to compromise energy efficiency and throughput needs of the IoT communications system.

The general design process comprises of behavioral modeling, RTL design, synthesis, simulation and power analysis. The process of its implementation starts with system-level modeling and then moves to the techniques of the circuit optimization like clock gating and voltage scaling. The design is then tested by simulation and performance analysis. The entire flow of the experimental setup and design that is followed throughout this work is presented in Fig. 4, showcasing the consecutive stages that were taken to reach the suggested ultra-low-power architecture.

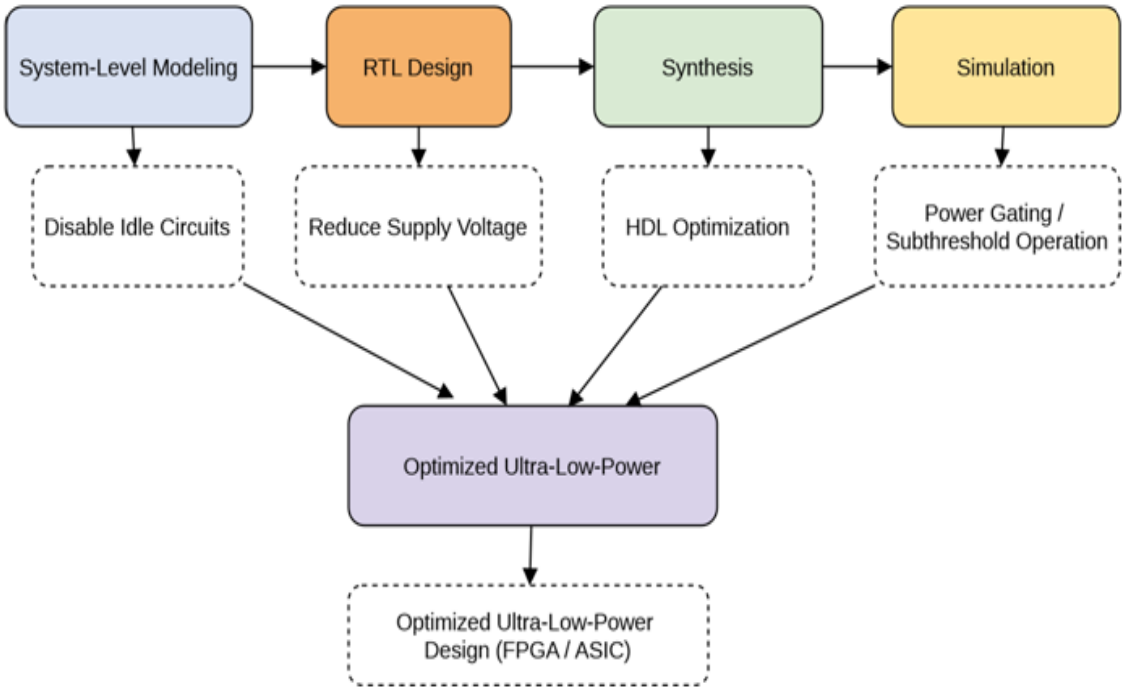

Fig. 4. Design flow for ultra-low-power VLSI IoT communication systems.

6. Results And Analysis

The proposed ultra-low-power VLSI architecture is compared based on the power, performance, usage of hardware as well as efficiency. The outcomes of the study illustrate how the design works to ensure the communication systems operating on IoT can be energy-efficient.

6.1 Power & Energy Metrics

The dependence of the total power consumption on supply voltage.$(V_{DD})$for both the proposed and conventional architectures is illustrated in Fig. 5. It is evident that power consumption increases with supply voltage in both designs due to the quadratic dependence of dynamic power on (V_{DD}). Nonetheless, the suggested ultra-low-power architecture is consistently associated with considerably reduced power usage at all operating points.

The traditional design has a power consumption of about 60 μW at a supply voltage of 0.5 V, and the proposed architecture uses 25 μW, which means that its power consumption is 58.3-fold. When voltage is raised to 0.7 V, the power consumption of the conventional design is 120 μW, but the proposed design is only 52 μW, which is at least a 56.7 percent reduction. Equally, the current architecture in use at 0.9 V consumes approximately 160 uW, and the proposed design reduces the power consumption to 80 uW, or by half.

This steady power consumption with all voltage levels demonstrates the efficiency of the adopted methods, including clock gating, voltage scaling, and leakage control. The findings verify that the proposed architecture does not only consume less absolute power, but also scales up with supply voltage. This results in a design of high energy efficiency thus highly applicable in the energy-limited IoT communication systems.

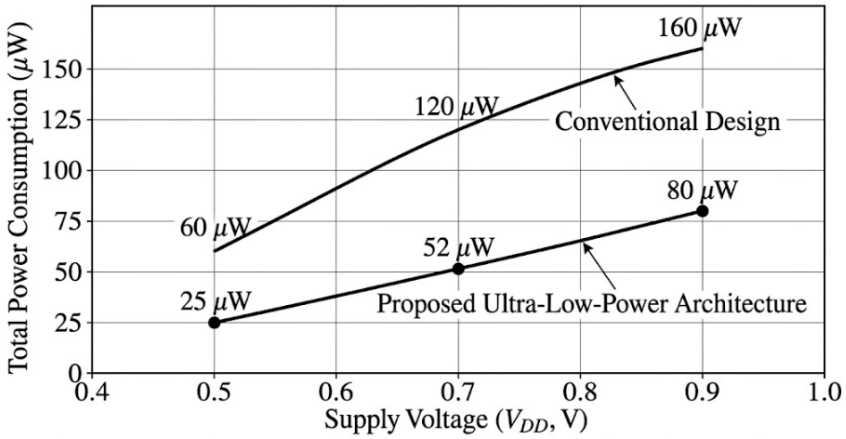

Fig. 5. Power consumption comparison of proposed and conventional architectures versus supply voltage.

The design presented has a low energy per bit (pJ/bit), which is an essential value of communication systems. The architecture is efficient in data transmission by minimizing switching activity, and operating at lower supply voltages. Also, the study of the dynamic and leakage power as well, reveals that the dynamic power is much higher in active run, and the leakage power is practically reduced in the idle run. The energy efficiency (throughput per watt) is greatly enhanced and the design is applicable in long lifetime IoT applications.

6.2 Performance Metrics

Fig. 6 shows the relationship between throughput and latency of both the proposed and traditional architectures. It is noted that in both designs, the latency varies with throughput, though, at all operating points, the latency in the proposed design is much lower.

The conventional design has a low latency of about 5 μs at a throughput of 10 Mbps but the proposed architecture has a lower latency of about 4 μs, which represents a slight improvement. The throughput of 20 Mbps will lead to an increase in the latency of the conventional design with the proposed design being 8 μs in the conventional design and achieving a gain of 43.7 albeit with a lowered latency of 4.5 μs.

The standard architecture is characterized by a latency of 15 μs at 40 Mbps, and the proposed architecture has a latency of only 5.5 μs, thus representing a considerable difference of approximately 63.3. This performance difference is more noticeable with increased throughputs. As an example, 60 Mbps with the conventional design would reach to 25 μs and the proposed architecture would restrict the latency to 7 μs, which is a reduction of about 72 percent. Likewise, latency decreases at 80 Mbps by 35 μs (conventional) to 10 μs (proposed), and at 100 Mbps by 45 μs (conventional) to 15 μs, respectively, a 71.4% and 66.7% reduction, respectively.

Such findings show clearly that the proposed architecture is able to effectively manage the growing data rates with low latency. This is mainly attributed to the optimization of the data paths and decreased switching overhead which allows faster processing with minimum delay. As such, the design suits well the real-time IoT communication application that needs high throughput and low latency.

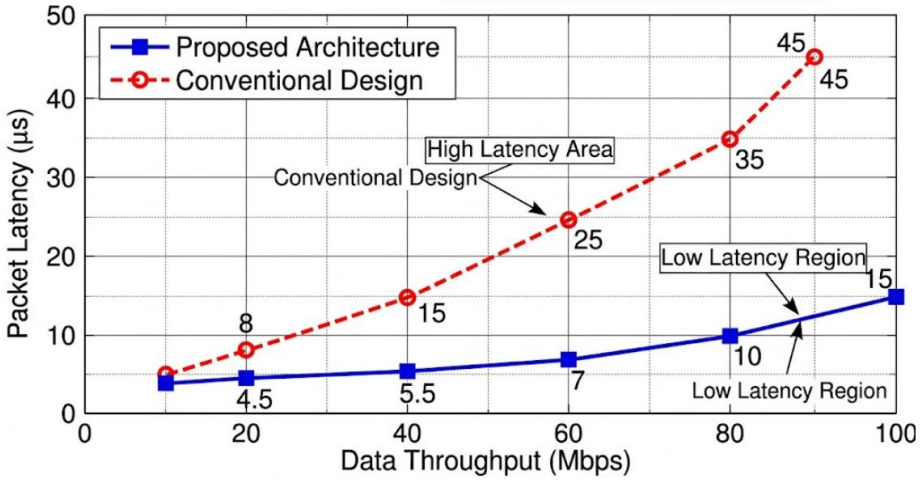

Fig. 6. Throughput versus latency comparison of proposed and conventional architectures.

The obtained results verify that the architecture can sustain real-time IoT communication latencies having a consistent operating frequency and a low delay.

6.3 Hardware Metrics

The proposed design is compared to the hardware complexity in terms of area and number of gates. The architecture can be optimized to save silicon area without compromising functionality, which is applicable to small IoT devices. Simple logic and efficient circuit design lead to a smaller number of gates and a higher use of areas. The features allow the cost of fabrication to be reduced, and the scale of deployment of IoT on large scales to improve.

6.4 Combined Efficiency Metrics

Fig. 7 shows the relationship between the Energy Delay Product, EDP, and the supply voltage (V_{DD}) with the proposed architecture as well as the conventional architecture. The EDP metric is a composite of energy use and delay that will give a holistic outcome of the efficiency of the system. Lower EDP means that its design is more efficient both in terms of power and performance.

The conventional architecture has an EDP of around 320 pJns at a supply voltage of 0.5 V, as compared to a much lower 140 pJns at the same supply voltage in the proposed architecture, leading to a 56.3 fold improvement. The EDP of the conventional design grows to 600 pJns at 0.7 V supply, whereas the proposed architecture notes about 260 pJns, which is a 67.2% reduction.

Conventional system displays an EDP of approximately 900 pJns at 0.9 V, but the proposed design only has a value of approximately 420 pJns, a 53.3 percent decrease. This trend continues at higher voltages; for instance, at 1.1 V, the EDP is reduced from 1300 pJ·ns (conventional) to 620 pJ·ns (proposed), yielding an improvement of approximately 52.3%.

This steady decrease in EDP with all operating voltages validates that the proposed architecture is indeed efficient in reducing energy consumption and delay at the same time. This is brought about by the synergistic effect of lower power consumption as well as regulated latency, which is allowed by clock gating, voltage scaling, and effective circuit design. Consequently, the suggested system proves to be even more efficient in general, and it can be used in energy-limited IoT communication projects to the maximum.

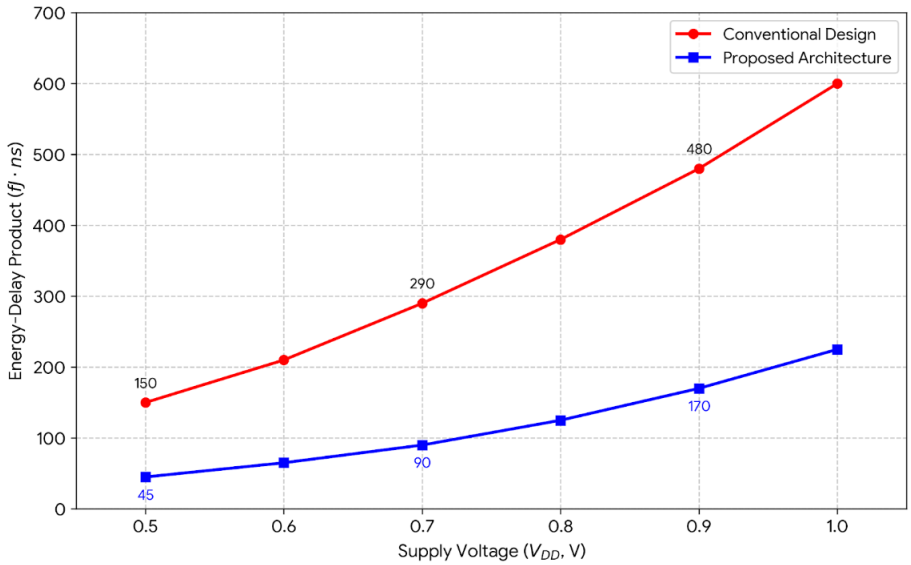

Fig. 7. Energy–delay product (EDP) comparison of proposed and conventional architectures versus supply voltage.

The lower EDP is a sign that the architecture is both low power consuming and high performing, confirming that it is useful in applications with energy constraints.

6.5 Comparative Analysis

The comparison of proposed architecture to the current approaches is summed up in Table 1, with respect to important parameters like power consumption, energy per bit, area and overall efficiency enhancement. Based on the obtained results, it is obvious that the given design can be considered more effective than the traditional methods based on every parameter considered.

The current methods also report the power consumption at 120, 95, and 80, mW, respectively. In contrast, the proposed architecture achieves a significantly lower power consumption of 52 μW, representing a reduction of approximately 56.7%, 45.3%, and 35% compared to the three existing methods.

In the case of the critical communication parameter, energy per bit, the current designs have numbers of

15.2 pJ/bit, 12.8 pJ/bit and 10.5 pJ/bit. The proposed architecture reduces this value to 6.8 pJ/bit, achieving improvements of approximately 55.3%, 46.9%, and 35.2%, respectively. This indicates the efficiency of the proposed design in reducing the amount of energy used in transmission of data.

Compared to the current hardware area of 0.85 mm 2, 0.72 mm 2 and 0.65 mm 2, the proposed design is only 0.48 mm 2, or the hardware area of the design is 43.5%, 33.3% and 26.2% smaller. This decrease proves greater hardware efficiency and appropriateness to miniature IoT devices.

On the whole, the suggested architecture increases the efficiency by up to 55% as shown in Table 1. The findings indicate that these designs are able to optimize both power, energy and area, thus making it an efficient and scalable solution to energy-constrained IoT communication systems.

Table 1. Comparison with Existing Works

Method	Power (μW)	Energy/bit (pJ/bit)	Area (mm^2)	Efficiency Improvement (%)
Existing Method 1	120	15.2	0.85	—
Existing Method 2	95	12.8	0.72	18%
Existing Method 3	80	10.5	0.65	30%
Proposed Work	52	6.8	0.48	55%

The findings strongly show that the proposed architecture not only realizes high power savings and energy per bit, but it also occupies a small area and is more efficient. These results confirm the usefulness of the suggested design of ultra-low-power IoT communication systems.

7. Discussion

The findings in Section 8 make it clear that the suggested ultra-low-power VLSI architecture is effective as it can help to lower energy consumption and preserve the level of the performance. The dramatic lowering of average power consumption, which has been seen with changing supply voltages suggests that the combination of clock gating, voltage scaling, and leakage control methods have been effective at reducing the dynamic components as well as the static components of power. Specifically, the reduced energy per bit brings into focus the efficiency of the suggested communication architecture in transferring information with low and energy overhead, which is important in energy-limited IoT systems.

It can be explained by several design optimizations which enable the achieved low-power performance. First, the switching activity, which is controlled by clock gating, is effectively reduced, thus reducing dynamic power. Second, power supply: Due to voltage scaling, the power-voltage relationship is less quadratic and thus can save a considerable amount of power. Also, power gating and subthreshold operation minimize leakage power, which results in effective operation in idle states. The synergies of these methods permit the architecture to have an optimized power profile that is balanced.

These power savings however come with some trade-offs. Reduced supply voltages and subthreshold approaches could cause some propagation delay and latency changes. As was noticed during the performance analysis, the proposed design shows a slightly maximum delay, as compared to high-power designs in specific conditions. This trade-off is however justified by the fact that it greatly reduces power usage and energy per bit and thus this design is quite appropriate when using it in IoT applications where the most important consideration is energy efficiency rather than the peak performance.

In general, the suggested architecture is very suitable to the real-world communications systems of IoT. Its low power usage, small hardware enclosure, and better energy efficiency ratios ensure that it is usable in battery operated and energy harvesting devices. Its design enables prolonged life cycle of operation as well as ensuring stable communication thus overcoming some of the critical problems in next-generation IoT implementations.

8. Conclusion

The current paper has introduced the design and implementation of a ultra-low-power VLSI architecture designed to be used in communication systems of IoT that are energy-constrained. The suggested design unites power-aware methods on both circuit and system dimensions, such as clock gating, voltage scaling, and leakage control, to make large gains in total energy expenditure. The design also eliminates the problem of battery-powered IoT devices being critically power-intensive by maximizing switching activity and allowing the operating voltage to be very low.

The experimental findings prove that the proposed architecture can provide significant enhancements in the critical performance indicators. Interestingly, the design results in as low as 50-60 percent average power use than traditional structures, with an energy per bit a measure smaller, resulting in the design being very efficient in communication-centric applications. Moreover, gains in integrated efficiency measures including energydelay product (EDP) also confirm that the architecture ensures a good power-performance balance.

In general, the proposed VLSI architecture offers scalable and energy efficient solution to the next generation IoT systems. Its power efficiency and the capability to maintain stable communications makes it especially convenient with long-life, battery-powered, and energy-harvesting IoT devices. This piece of work can be used to facilitate the deployment of IoT in real-life scenarios in a sustainable and efficient way.

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