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RESEARCH ARTICLE

# Design and Performance Optimization of an Energy-Efficient VLSI Architecture for Low-Power Embedded Computing Systems

**M. Kavitha***

*Department of ECE, Saveetha School of Engineering, Saveetha Institute of Medical and Technical Sciences, Saveetha University, Chennai, India*

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## Abstract

The energy-efficient VLSI architectures are in urgent demand due to the high-rate of increasing low-power embedded computing systems in Internet of things (IoT) systems, wearable devices, and edge intelligence. Philosophical design Traditional designs are constrained by excessive high dynamic switching power and growing leakage currents, especially in deep submicron process technologies, which worsen energy efficiency significantly. In this paper, the design and performance optimization of a low power VLSI architecture incorporating dynamic voltage scaling (DVFS), frequency scaling, as well as adaptive power gating, is described within a single workload-conscious control system. The suggested architecture manages supply voltage and operating frequency dynamically according to the actual workload conditions in real-time and nonquite completes on power gating of idle circuit blocks by using sleep transistor. Dynamic and leakage power components are analysed using a comprehensive mathematical model and optimising the overall energy consumption at the circuit level is utilised. The architecture would be tested by simulation with 45 nm CMOS technology model in different scenarios with changing workload. Findings show significant advances such as low power draw, low energy-delay product and kept low latency as opposed to traditional and DVFS-only styles. The planned design presents an efficient, scalable and practical model in energy-restricted computing avenues in forthcoming low-power embedded systems.

**Author's e-mail:** kavithamece@gmail.com

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## Introduction

The high rate of adoption of embedded computing systems in Internet of Things (IoT), smart healthcare, edge intelligence systems have intensely amplified the requirement of energy efficient hardware. The systems are often very strict on power, thermal, and resource constraints, and thus energy optimization is not an additional consideration, but rather a core issue of design. VLSI designs are now vital to making embedded computation high performance, but, unfortunately, the existing designs are typically designed to be fast and small with the costs of power-aware operation rarely considered, thus resulting in inefficient energy usage in contemporary applications.[1, 2] In present-day CMOS technologies, the total power consumption is dominated by dynamic as well as leakage components. Switching activity and capacitive charging are

the major contributors to dynamic power, but subthreshold conduction and leakage currents to the gate oxide through leakage currents are considered the largest contributors to leakage power, and become increasingly important in deep submicron nodes.[3, 4] Dynamic Voltage and Frequency Scaling (DVFS) has also been commonly used to provide dynamic power savings by scaling supply voltage and clock frequency based on the workload conditions. Nonetheless, DVFS cannot be effective in the process of leaking power reduction in the idle or low-activity mode. In contrast, those power gating mechanisms can successfully minimise the leakage through the inactivation of non-active circuit blocks however, they could add to the delay at the time of waking up and to the overhead of controls unless managed properly.[5, 6] Recent studies have examined hybrid techniques of power management with a mix of DVFS and power gating. Nevertheless, most of the current solutions do not have an integrated method of dynamically coordinating the two techniques using a workload-aware control mechanism. Also, some of the designs lack circuit-level validation and the effective balance between energy efficiency and performance, which restricts their use in real-world embedded systems.[7, 8]

As a solution to all these shortcomings this paper suggests a hybrid energy efficient VLSI that combines the DVFS with adaptive power gating into a common control platform. The system proposed uses workload-aware controller to dynamically control operating voltage, frequency and activity of the modules, which helps in controlling dynamic power consumption, leakage power consumption and performance optimism. Power behaviour is modelled mathematically and analysis of the design is provided at the circuit level to allow practical feasibility. The primary contributions of the work are as follows: development of power-aware VLSI architecture, combining adaptive DVFS and power gating, creation of analytical power models and simulation of system performance under different workload conditions.

## Related Work

A significant area of research interest has been energy efficient VLSI design as the power available in more modern edge computing and embedded systems steadily grows lower. One successful approach to the minimization of dynamic power consumption is Dynamic Voltage and Frequency Scaling (DVFS) which is one of the techniques deeply-rooted in the dynamical power consumption reduction approaches involving the adjustment of the supply voltage and clock frequency based on the workload requirements. It has been shown in the previous studies that DVFS can greatly decrease switching power, but in deep submicron technologies where leaks become predominant, it is not effective.[9, 10] In order to solve the leakage power, it has been proposed to use power gating methods, where idle blocks of a circuit are disconnected by using sleep transistors to disconnect the power supply. These techniques are useful to minimise the leakage currents during standby as well as enhance energy efficiency. Nevertheless, the emergence of sleep transistors causes some problems like the latency to wake up, state retentions, and complexities in designing transistors and this trouble could reverse the system functioning unless critical optimization is done .[11, 12] Authors have attempted to initiate research that investigates possibilities of hybrid methods that can be developed by integrating DVFS and power gating to pursue holistic power optimization in recent studies. As an example, synchronised power management systems have been suggested to enable the dynamic optimality of voltage scaling, as well as the anactivation of modules, depending on the workload. Although they are more energy efficient, most of them do not include a single and intelligent control mechanism, which could realise real-time trade-off between performance and power consumption thus resulting in suboptimal performance, as far as power consumption is concerned.[3, 4] Moreover, some present literature is entirely based on algorithmic level or architecture level optimization without giving the circuit-level implementation and justification. This reduces their real-world feasibility in actual-life VLSI systems, in which circuit level factors are very important to the overall performance and reliability.[5]

Unlike other algorithms, this project suggests a scalable and workload-sensitive VLSI design, which incorporates DVFS and adaptive power gating in a single management environment. The proposed solution focuses on architectural efficiency as well as circuit-level implementation, and this allows to reduce efficiently dynamic and leakage power and retain system performance.

## Proposed Methodology

The study in this paper dwells upon the systematic design and performance optimization of an energy efficient VLSI architecture by incorporating dynamic voltage and frequency scaling (DVFS) and adaptive power gating using a common control platform. The methodology is built to solve both dynamic and leakage power, which is the most significant source of energy ineffectiveness in the present embedded system of CMOS-based embedded systems. The given approach is designed in such a way that it consists of four interdependent steps, i.e. architecture design, analytical power modelling, circuit-level implementation, and simulation-based performance evaluation. All of these stages allow the comprehensive exploration of power-performance trade-off in different conditions of workload.

## Architecture Design

The design phase of architecture forms the basics of the suggested system by providing a modular and versatile VLSI framework. The architecture is made up of four main elements, namely processing core, which performs computational functions, DVFS controller, which is used to dynamic regulation of voltage and frequency, power gating unit that enables reduction of leakage power and the workload-adaptive control unit, which coordinates the systems behaviour, which is shown in Fig. 1. The research methodology involves designing of a mechanism of workload monitoring integrated into the control unit. This unit is constantly assessing the activity of systems in terms of the execution patterns of tasks and resource use. With the aid of this analysis, it identifies the best mode of operation of the system. Under low workload scenarios a control unit causes the DVFS controller to decrease the supply voltage and clock frequency to decrease dynamic power consumption. At the same time, it has the effect of power gating unit(s) to put out dynamically inactive modules with sleep transistors, which practically reduce leakage currents. Conversely, the system recovers full voltage and frequency levels when high-computational demand is detected and retains the performance. The dynamics between DVFS and power gating is well orchestrated so as not to cause any loss in performance but to create smooth transitions between operation states. It is applicable in real-time embedded systems by making it an efficient management of energy within a broad-based application location.

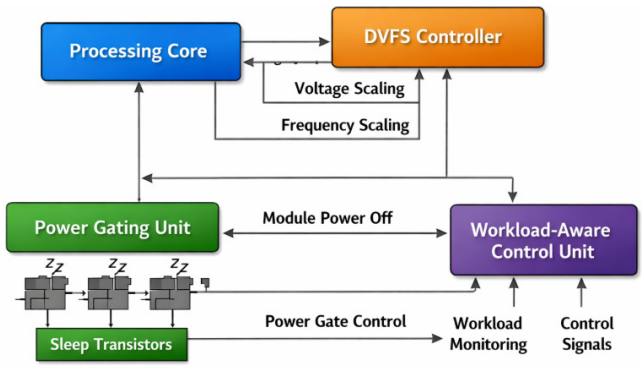


**Fig. 1: Proposed VLSI architecture illustrating integration of DVFS and power gating mechanisms.**

## Power Modeling

In order to measure the efficiency of the proposed architecture quantitatively, mathematical model of power consumption is established. The total power is represented in the CMOS based system as the dynamic power consumption and leakage power consumption which are investigated independently to gain knowledge of their respective contributions to the overall power-consumption. This is as a result of dynamic power consumption is modelled in terms of switching activity and capacitive loading which is given by:

$$P_{dynamic} = \alpha C V^2 f \quad (1)$$

In which the switching activity factor is the determinant of the rate of signal transitions, the load capacitance is the physical properties of the circuit, the power is dependent on the supply voltage in quadratic terms, and the rate of computation is determined by the operating frequency. The effectiveness of DVFS that is evidenced by this relationship is that the lower the voltage and frequency, the large decreases that can be achieved in the dynamic power.

Leakage power is modeled as:

$$P_{leakage} = I_{leak} \cdot V \quad (2)$$

In which the leakage current takes into consideration the subthreshold conduction and gate oxide leakage effects that is prevalent in scaled technologies. The suggested methodology minimises the leakage power, it uses power gating that isolates the idle circuits blocks with reference to power supply.

The study also contrasts system efficiency in terms of energy-delay product (EDP) that gives in all round measure balancing between energy usage and computational ability. With this modelling framework, it is possible to accurately determine the effect of the architectural and circuit-level optimizations.

## Circuit-Level Implementation

After the architectural and analytical design, the suggested methodology will use the circuit-level implementation to guarantee the practical feasibility. This phase is concerned with the mapping of the conceptual design into hardware level designs which are feasible to implement using CMOS technology. Implementing the power gating mechanism is a matter of a few sleep transistors in between the blocks of logic and the power supply as shown in Fig. 2. These transistors are switches that are governed by work load aware unit. When the system goes idle, the sleep transistor is switched off basically isolating the circuit thus greatly minimising leakage currents. When the transistor is in active operation, it is an active transistor and it is switched on to restore normal current flow to it and it works back to its full capacity. The placement and size of sleep transistors have been carefully sized and placed to ensure that the voltage drop and switching delay is minimal. The DVFS system is realised by using programmable voltage regulators and clock scaling circuits. The supply voltage is dynamically changed by the voltage regulator and

operating frequency changed by the clock scaling unit in reaction to the workload changes. This coordination among these components is done by the use of control signals generated by the workload-conscious unit so that power gating and DVFS functions in sync. This circuit implementation confirms the feasibility of the given architecture and yields that the hypothetical benefit of the power consumption is practically realisable in actual hardware designs.

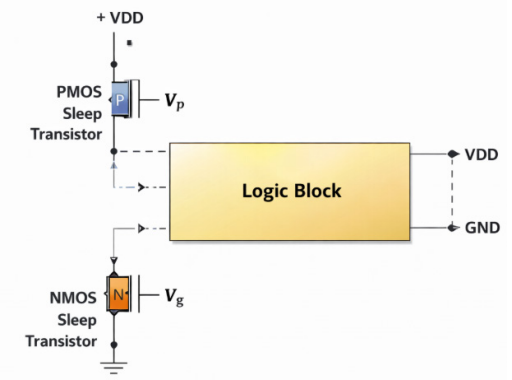


**Fig. 2. Power gating circuit illustrating sleep transistor-based leakage power reduction mechanism.**

### Simulation Setup

In order to test the efficiency of the suggested methodology, one considers the analysis of the simulation through simulation tools, including Cadence and MATLAB, which is the industry standard. Design is modelled in a 45 nm CMOS technology node that is also realistic to the current embedded systems. The simulation environment will be configured in such a way that it evaluates the system behaviour when it is exposed to different work load conditions so as to have a thorough assessment of the energy efficiency and performance. Among the important parameters that are manipulated in practical limits to determine effectiveness of DVFS are supply voltage, operating frequency among other parameters. Also, the workload intensity is also dynamically varying to test the ability of the control unit and compliance of architecture. The performance measurements such total power consumption, latency, energy efficiency, and energy- delay product are measured and compared to the Netflix architecture of baseline architectures, including conventional VLSI systems, and DVFS-only implementations. With the help of this comparative analysis, the benefits of the proposed methodology can be easily shown. The obtained outcomes of the simulation procedure in question lend quantitative support to the idea in question and indicate that the suggested strategy is going to help cut power consumption, though without sacrificing performance when it comes to a wide range of operating situations.

## Results and Discussion

Simulation is used to investigate the performance of the proposed energy efficient VLSI architecture under different workload requirements, supply voltages and operating frequencies. The findings are contrasted with the traditional VLSI design and the DVFS-based design to prove the efficiency of the new approach.

### Power Consumption Analysis

Fig. 3 shows the dependency of the total power consumption on the operating frequency. It is noted that the proposed architecture attains a considerable drop in the consumption of power at all levels of frequency. This is due to the synergies of DVFS and power gating wherein DVFS minimises dynamic power consumption by scaling back voltage and frequency and power gating that minimises idle leakages. In comparison to the traditional designs, the offered system can achieve about 25-40% less total power consumption, especially in low and moderate workload conditions.

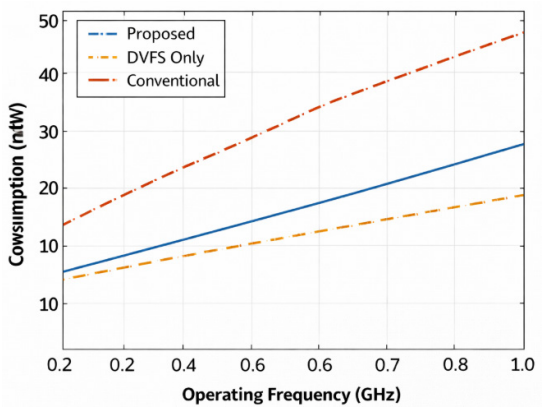


**Fig. 3: Power Consumption vs. Operating Frequency for Different VLSI Architectures**

### Latency Analysis

Fig. 4 presents the performance of the proposed architecture in terms of latency when the workload is varied by different levels of intensity. The findings show that the system has low latency even when it is working with low voltage and frequency. This is done by effective workload-sensitive control guaranteeing performance critical modules to stay live. This is in contrast to any conventional power-saving mechanism that may cause severe performance reduction; the method proposed does not cause any drastic reduction in the performance, hence, the latency overhead is only relatively high as compared to running at full-performance.

### Energy Efficiency Evaluation

Fig. 5 provides the energy conservation of the proposed architecture compared to those of conventional systems

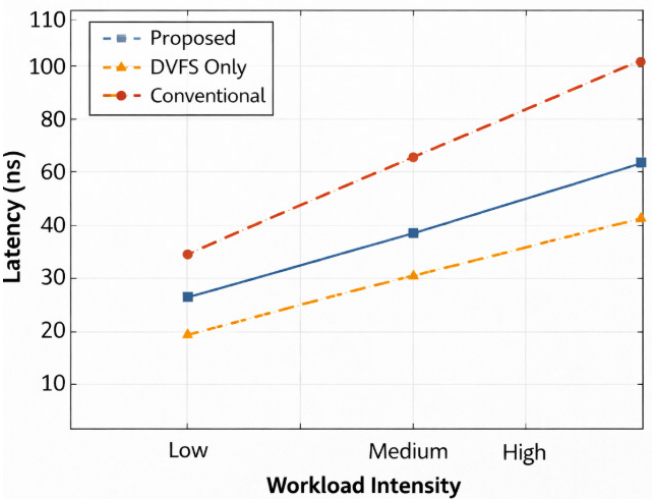


**Fig. 4: Latency vs. Workload Intensity for Proposed and Existing Architectures**

and DVFS-only. The findings indicate that the proposed architecture is more energy efficient because it has an optimised utilisation of the resources and also offers better coordination between DVFS and power gating. Embedded applications with limitation in energy availability can effectively use the system as the increase in energy consumption is estimated at 30-45 percent.

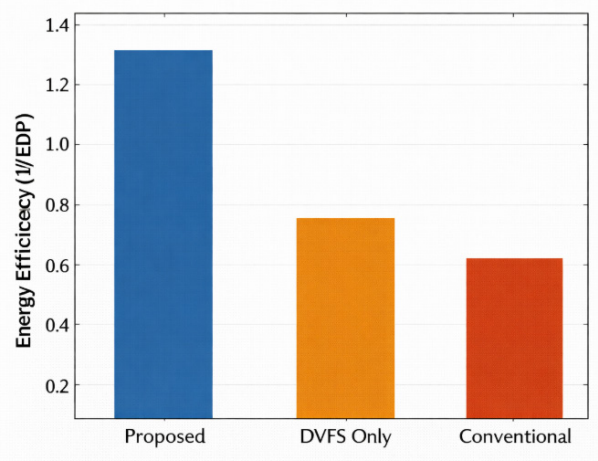


**Fig. 5: Energy Efficiency Comparison Among Proposed, DVFS-Only, and Conventional Architectures**

### Energy-Delay Product (EDP) Analysis

Fig. 6 analyses the energy-delay product that is the trade-off between power consumption and performance. The architecture proposed has the lowest EDP among all compared methodologies, which means that it has the best balance between energy saving and speed. It is mainly because of the adaptive control mechanism through which the operating parameters are adjusted dynamically in response to the conditions of the workload.

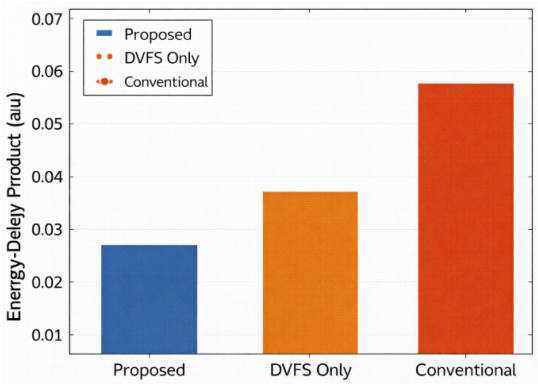


**Fig. 6. Energy-Delay Product Comparison for Proposed, DVFS-Only, and Conventional VLSI Architectures**

### Comparative Discussion

The proposed methodology is a more dynamic and versatile power management solution compared to the current techniques that make use of DVFS and power gating (only). Past works have been shown to either enhance both dynamic and leakage power or to only in one of the two, and have no real-time adaptability. Conversely, the proposed architecture also incorporates both methods in a single control system which leads to higher levels of scalability, less power usage and more stable performance levels.

In general, the findings validate that the developmental VLSI architecture is a definite breakthrough in the energy-efficient design, and would therefore be very applicable in the next generation embedded computing systems, such as the IoT and edge-based computers.

## Conclusion

In this paper, internal architecture design and optimization of performance of a hybrid energy-efficient VLSI architecture optimised to low-power embedded computing systems has been provided. The given solution combines the idea of dynamic voltage and frequency scaling (DVFS) with dynamic adaptive power gating on a single workload-aware control system to consider the dynamic and leakage parts of power. The proposed architecture allows real-time adaptation of these techniques to coordinate their work, unlike traditional methods that exploit these tools separately, thus, leading to the achievement of better energy-performance efficiency. The modelling of analytical power and the practical feasibility of the design is guaranteed by the introduction of a model of the analytical power and its practical implementation on the circuit level. The results of the simulation indicate that the proposed architecture obtains significant cutbacks in total power consumption and energy-delay product with a low latency in a range of working load conditions. The above improvements address

how efficient the suggested methodology is in reaching the balance between computational performance and energy efficiency. The proposed architecture provides a flexible and strong implementation of the next-generation embedded systems, especially in energy-restrictions structures like IoT and edge computing platforms. Future directions will be dedicated to hardware implementation with the help of FPGA-based prototypes to check the performance of real-time, and the implementation of machine learning-based predictive control systems on predictive power management. Moreover, the design can be extended to high-technology nodes and non-homogeneous designs, which also will be a good colour of possible future energy efficiency of the upcoming computing systems.

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