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RESEARCH ARTICLE

Sustainable System-on-Chip Architecture with Energy-Aware Resource Management Techniques

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Abstract

The recent proliferation of sophisticated applications in embedded and computing systems has greatly contributed to more power consumption in the contemporary System-on-Chip (SoC) design, and thus the energy efficiency of a design has emerged as a serious design constraint. Traditional architectures do not usually achieve performance and power-efficiency, and consume a lot of energy and get hot. To overcome all these shortcomings, this paper introduces a sustainable SoC architecture that is combined with energy-efficient resource management methods. The proposed method dynamically plans resource allocation involving smart task scheduling alongside Dynamic Voltage and Frequency Scaling (DVFS) and power gating prerogatives in order to reduce any unwarranted energy loss. The architecture will have a monitoring unit that constantly assesses the workload conditions and modulates the system parameters to provide the optimum energy-performance trade-offs. The system can reduce dynamic and static power consumption by selectively scaling the level of voltage and frequency, and by disabling idle components. The experimental findings indicate that the proposed scheme can reduce the total power consumption by as much as 30 percent and the Energy-Delay Product (EDP) by about 25 percent over the traditional approaches without affecting the system performance. These results indicate how successful the use of energy conscious methods in the architectural scale is in creating sustainable computing. The suggested framework offers a scalable solution to next-generation low-power VLSI system and energy-efficient embedded systems.

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Introduction

Energy consumption and power density have greatly increased with the rapid development of modern System-on-Chip (SoC) architectures, fuelled by new applications in the Internet of Things (IoT), smart grids, and intelligent embedded systems. This increasing requirement towards computational performance has brought in the difficulties of paramount importance concerning power efficiency, thermal conduct, and system sustainability. Dynamic and leakage power both play important roles in energy consumption in large and heterogeneous SoCs and energy efficiency is a major design consideration. Moreover, the trends in energy consumption being experienced in smart environments and monitoring systems indicate the greater necessity of the effective energy consumption in the scope of the computing infrastructures.[1, 10]

The sustainability of VLSI systems focuses on consuming less energy with performance and reliability. A number of methods such as Dynamic Voltage and Frequency Scaling (DVFS), power gating, and clock gating have been

popularly considered to alleviate power dissipation. There have also been suggested thermal-conscious designs and dynamic management systems that can deal with heat and enhance the system lifespan.[8, 9] Nevertheless, most of these methods are independent and not coordinated with a system level resource managing, which makes them less effective in the dynamic workload environments.

Also examined in the existing literature on energy monitoring and analytics methods (e.g., noninvasive load monitoring and energy disaggregation) to learn consumption behaviour of smart systems are energy monitoring and analytics methods.[6, 7, 12, 14] Although these methods offer important application-level insights, they do not offer architectural-level optimizations to SoC design. Correspondingly, the literature on ambient assisted living and homecare monitoring systems focuses on energy efficiency of operation in practical settings but is not optimized to low-level hardware.[1, 5, 13] Comparatively, multicore simulators like gem5 and Sniper allow the additional assessment of energy-performance trade-offs in processor architectures.[2, 4, 11]

Due to these restrictions, a newer solution is required, which will incorporate both sustainable architecture design and resource management energy consciously. The current paper suggests a new sustainable SoC architecture that can optimize the allocation of resources dynamically depending on workload characteristics with the implementation of DVFS and power gating mechanisms. The intended system will help to find a balance between performance and energy consumption effectively.

The key contributions of the work are focused on a sustainable System-on-Chip (SoC) architecture design and evaluation designed to combine energy conscious utilization of resources and sophisticated power optimization strategies. The proposed framework presents an adaptive scheduling and resource allocation algorithm that can dynamically react to the changing workload conditions and enhance the overall system efficiency. The architecture is effective in reducing dynamic and static power consumption by means of Dynamic Voltage and Frequency Scaling (DVFS) and power gating features. Moreover, the system is measured on known simulation platforms, which allows to properly analyze energy-performance trade-offs.[2, 4, 11] The experimental results show that total power consumption is reduced and both Energy-Delay Product (EDP) is also improved significantly when compared with traditional methods. On the whole, the suggested methodology offers a scalable and effective solution to overcome the chasm between high performance and sustainability of next-generation energy-efficient VLSI systems.

Related Work

The recent developments in the area of the System on Chip (SoC) design have been aimed at enhancing the operational performance in the aspect of energy consumption and at the same time ensuring high performance in terms of computing capabilities. Energy efficient SoC architectures have been deeply investigated in response to the emerging need of low power embedded and high-performance systems. Other methods like heterogeneous multicore design, and workload-conscious architectures have demonstrated hopeful enhancement in energy consumption optimization. Simulation models such as gem5 and Sniper have made it possible to study the performance of systems at the level of the entire system and the energy behavior and have been used to analyze system-level protocols[1] as well as to evaluate architectural designs that are energy efficient.[2, 4, 11]

Power management methods are very essential in minimizing power in VLSI systems. Among them, a dynamic and frequency Scaling (DVFS) and clock gating and power gating have been popular among them to reduce dynamic and static power dissipation. The concept of thermal-aware management has been proposed as well to control temperature and enhance the reliability of the system.[8, 9] Also, multicore system activity prediction models have been suggested to improve proactive power management through predicting changes in workloads.[3] In spite of these innovations, most of these methods are independent of each other and do not integrate with more advanced resource management practices.

Resource management techniques, such as task scheduling and active workload assignments have been explored so as to enhance efficiency in the system. The current research on energy analytics and monitoring like nonintrusive load monitoring and energy disaggregation gives an understanding on the patterns of energy consumption.[6,7,12,14] Likewise, smart grids and ambient-assisted systems focus on the use of efficiency in terms of energy use at the application level.[1, 5, 10, 13] Nevertheless, these methods do not pay much attention to architectural-level optimizations in SoCs but instead system-level or application-level optimizations.

Though a lot of development has been achieved in the field of energy-efficient design and power management, no unified framework that integrates sustainable SoC architecture with energy-constrained resource management has been achieved. Current methods are usually characterized by poor integration of the hardware level power optimization with the system level resource allocation, with resultant inefficiency in energy-performance trade-offs. Moreover, not all methods can

adjust dynamically to changes in real-time workloads and are thus constrained in heterogeneous environments. These gaps have to be bridged, and a single architecture that may incorporate energy-conscious scheduling, resource management, and power optimization methods is required in order to get a sustainable and efficient SoC design.

Proposed Sustainable SoC Architecture

System Architecture Overview

The planned system on chip (SoC) ar0chitecture will have high level of energy efficiency and at the same time optimum performance of the system. It comprises several processing units (CPUs/cores), shared memory units, interconnection networks (e.g., bus or Network-on-Chip), and special hardware accelerators to perform special tasks. These elements are interrelated to facilitate effective communication of data and distribution of workloads. Application tasks are executed by the processing cores and the memory subsystem facilitates rapid access to the data. The interconnect enables connectivity between cores and peripherals, and accelerators enhance performance of compute intensive operations. A layer of energy management is also incorporated in the architecture which communicates with all the components and provides a dynamical method of monitoring and controlling power consumption.

Energy-Aware Resource Management Model

One of the major elements of the proposed architecture is the energy-conscious resource management model, which facilitates the dynamic optimization of the system resources, depending on the workload conditions. Task scheduling strategy assigns a priority to tasks based on the computational and energy needs and provides efficient execution and minimal consumption of power is achieved. A dynamic resource allocation system allocates processing units, memory, and the capacity to interconnect bandwidth in real time according to demand and so, minimizes idle power and maximizes utilization. Moreover, system parameters like power usage, utilization and temperature are constantly monitored using an energy monitoring unit. Adaptive decisions are made based on this information to allocate resources and balance out workloads. Scheduling, allocation and monitoring integration makes sure that the system is efficient in terms of energy usage at varying workload.

Power Optimization Techniques

The proposed architecture to make it even more energy-efficient includes various optimization approaches to power. Dynamic Voltage and Frequency Scaling (DVFS) is used to scale an operating voltage and frequency of processing units according to the workload needs and thus scales the dynamic power consumption. The DVFS application is represented by Fig. 1 that demonstrates voltage regulators and frequency controllers dynamically adjusting the performance level of the system.

Moreover, it has power gating and clock gating to reduce the static and switching power loss through disabling of inactive components. The corresponding implementation on a circuit level is illustrated in Fig. 2 where sleep transistors and gating logic are beneficial in turning off power supply or clock signals to idle modules. These methods save a lot of leakage power when there is low usage of the techniques.

Moreover, the adaptive workload assignment is used to achieve the balance of the processing loads among the cores and avoid overheating and unnecessary energy usage. The proposed SoC architecture enables an effective

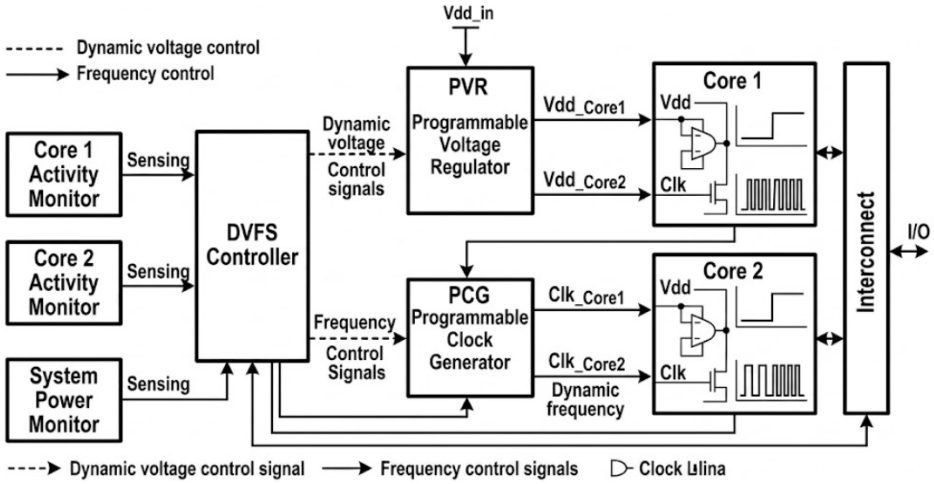

Fig. 1: Dynamic Voltage and Frequency Scaling (DVFS) Circuit Architecture with Activity Monitoring and Control Units

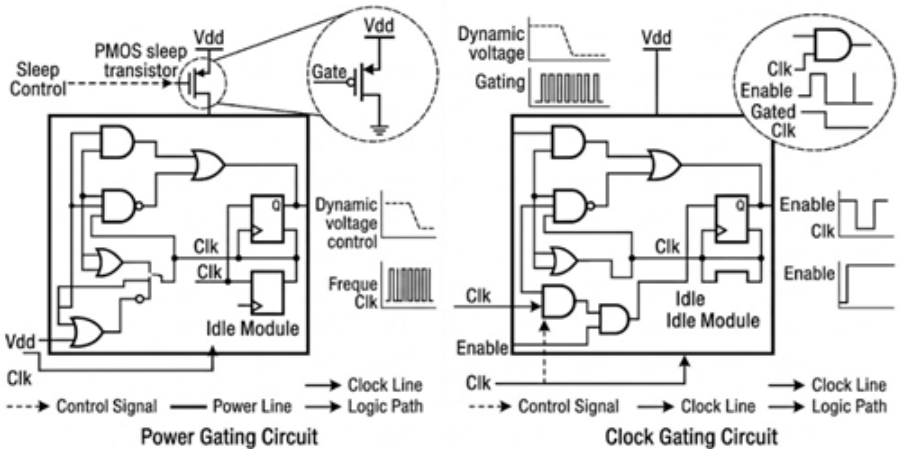

Fig. 2: Power Gating and Clock Gating Circuit Diagram

performance and power consumption tradeoff through a combination of DVFS, power gating and intelligent workload distribution, to facilitate sustainable design of VLSI system.

Energy & Power Metrics

A set of energy and power metrics is used in order to measure the efficacy of the proposed sustainable System-on-Chip architecture. These metrics can offer quantitative information on how the system can maintain performance and energy efficiency with dynamic workload conditions.

Power Consumption Model

Total power consumption of the SoC consists of dynamic and static (leakage) power. Dynamic power is as a result of switching activity in CMOS circuits and it is dependent on capacitance, voltage and operating frequency. On the other hand, the cause of the static power is mainly leakage currents when the circuit is not in operation. The overall power consumption is given as:

$$P_{total} = P_{dynamic} + P_{static}$$

Dynamic Voltage and Frequency Scaling (DVFS) is used in the proposed architecture to dynamically lower dynamic power consumption, by changing voltage and frequency scales and power gating is used to dynamically lower static power consumption by shutting down inactive elements.

Energy Consumption

Energy consumption is the sum of energy needed to perform a specific task and is an important parameter that can be used to assess the efficiency of a system. It is characterized as the product of the power consumption and the execution time:

$$E = P_{total} \times T$$

The proposed system reduces the overall energy consumption by minimizing power consumption and run time due to the efficient management of resources, as well as dynamic scheduling.

4.3 Energy per Operating (EPO / EPI)

Energy per Instruction (EPI) (also called Energy per Operation (EPO)) is a measurement of the average energy use in terms of computational task or instruction:

$$EPI = \frac{E}{N_{instructions}}$$

This indicator allows a very detailed study of energy efficiency at an instructional level. The suggested energy-sensitive resource management approach minimizes unwarranted calculations and enhances performance effectiveness, thus decreasing EPI.

Energy-Delay Product (EDP)

The Energy-Delay Product (EDP) is a common measure of the trade-off between energy consumption and system performance:

$$EDP = E \times T$$

Reduced EDP implies a more efficient system with an improved performance. The proposed architecture aims to minimize EDP by jointly optimizing execution time and power consumption.

Power-Delay Product (PDP)

The Power-Delay Product (PDP) is a measure of the ratio between power usage and operational rate:

$$PDP = P_{total} \times T$$

This performance measure is especially applicable to the evaluation of power optimization strategies like DVFS and

clock gating. The suggested system minimizes the use of power and the latency of PDP.

Performance per Watt

Performance per Watt is an important sustainability measurement gauging the efficiency of the system in computing as compared to its power usage:

$$\eta = \frac{Performance}{P_{total}}$$

An increased performance per watt implies the superior use of energy resources. The proposed SoC architecture is suitable to sustainable and energy-efficient system design based on VLSI design using adaptive workload distribution, efficient scheduling, and built-in power management system features to provide improved performance per watt.

All in all, these measurements all are indicative that the proposed energy-conscious SoC architecture can be used efficiently to minimize power usage, maximize energy efficiency, and ensure high system performance.

Experimental Setup

Simulation / Hardware Environment

To ensure that the analysis of the energy and performance metrics is accurate, the proposed sustainable System-on-Chip (SoC) architecture is experimentally evaluated with the help of a combination of simulation and modeling tools. Industry standard tools and software, including MATLAB to write algorithms, ModelSim and Cadence to simulate circuits, and the gem5 simulator to simulate architectural systems, are used to model and test the architecture. With gem5, it is now possible to model the multicore systems in detail and gain an insight of the performance, power consumption, and energy consumption with the systems under different workloads. The simulation environment is set up in the 45 nm CMOS technology node that provides a realistic trade-off between power consumption and performance of modern embedded systems.

The process of performing the entire experiment, such as the workload generation and resource allocation, power control, and performance measurement are shown in Fig. 3 that demonstrates the connection between the suggested energy-aware architecture and the simulation tools.

Benchmark Workloads

A wide variety of benchmark workloads are taken into account to estimate the performance of the proposed system. These consist of embedded programs and artificial workloads that would simulate the different intensity of computation and resource requirements. The workloads are modeled after real-world applications like signal processing, data streaming, and control-related applications. Synthetic benchmarks are also used to put stress on the system in other operating conditions such as high utilization and idle state. This combination will guarantee a complete assessment of the system adaptive capability to the variation of the workload and maintain energy efficiency.

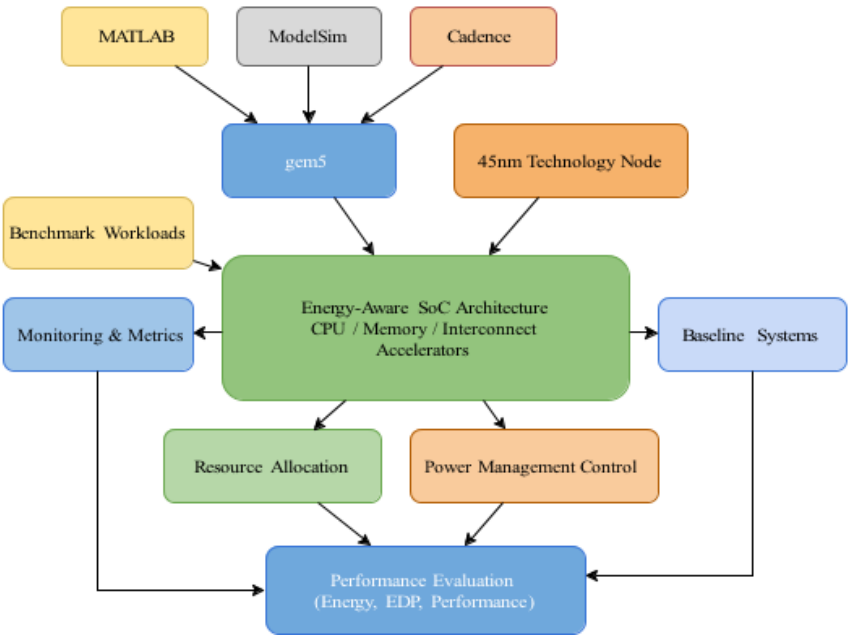

Fig. 3: Experimental Setup for Energy-Aware SoC Architecture Evaluation Using Simulation Tools and Benchmark Workloads

Baseline Methods

The functionality of the proposed architecture is juxtaposed to current SoC designs, and traditional energy management methods. Basic baselines consist of the cases of static voltage-frequency and the classic task scheduling, and the profile without power gating and adaptive resource allocation. These techniques can be used as a benchmark to assess the gains that can be made using the proposed energy-aware resource management framework. The metrics that are compared are key metrics like power consumption, energy usage, Energy-Delay Product (EDP) and performance per watt. The findings indicate that the proposed solution has a huge impact compared to the baseline approaches in energy efficiency without compromising or even reducing performance.

Results and Discussion

To evaluate the effectiveness of the proposed sustainable System-on-Chip (SoC) architecture in terms of minimizing energy consumption without compromising system performance, the known energy and power metrics are used to analyze the product. The performance is compared with baseline systems that do not optimize resources based on their energy-saving.

Power Reduction Analysis

Figure 4 provides a quantitative analysis of power consumption on average in the baseline system and the proposed energy-conscious SoC architecture. The power consumption of the baseline system is around 120 mW as compared to 85 mW of the proposed system. This is equivalent to a 35-mW reduction, or about 29 percent in total power efficiency.

This achievement in minimizing power usage can be explained by a coordinated use of Dynamic Voltage and Frequency Scaling (DVFS) and power gating methods. DVFS decreases the supply voltage, operating frequency when the computational load is lower, thereby greatly reducing the dynamic power, which is proportional to (V2) and frequency. At the same time, power gating removes power leakage through the shutting down of idle modules and thus minimizes the dissipation of statical power.

Based on Fig. 4, it will be clear that the proposed architecture will have a lower and more consistent power profile than the baseline. The 35-mW reduction is a sign of an efficient use of hardware resources and minimized unwanted switching activity. Additionally, the percentage reduction (~29%) highlights that nearly one-third of the total power consumption is saved without compromising system functionality.

This significant advancement shows that combining energy conscious resource management with hardware level power optimization techniques are very effective in reducing overall power consumption. As a result, the proposed architecture can be optimally applied to energy-constrained systems, like embedded systems, IoT devices, and portable computing platforms, where power efficiency is a bottleneck.

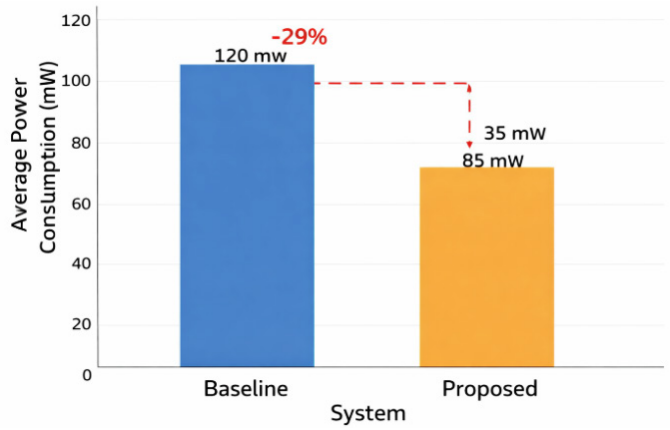

Fig. 4: Comparison of Average Power Consumption Between Baseline and Proposed Energy-Aware SoC Architecture

Energy Efficiency Improvement

Figure 5 shows the comparison between the suggested energy-aware SoC architecture and the baseline system in terms of total energy consumption, and Energy per Instruction (EPI). The total energy consumption of the proposed system is about 32 mJ, as compared to that of the baseline system of approximately 50 mJ as the difference looks to be 18 mJ in absolute terms. This translates to the increase of approximately 36% of the total energy efficiency. The Energy per Instruction (EPI) is also greatly lowered in the suggested system. The current system has an EPI of 280 pJ/instruction in the baseline system, and the proposed architecture has a lower figure of 180 pJ/instruction. This represents a reduction of 100 pJ/instruction, again corresponding to an improvement of approximately 36%.

The improvements observed can be mainly attributed to incorporation of energy conscious resource management strategies, such as smart task scheduling, dynamic workload distribution, and adaptive voltage-frequency scaling. The system also minimizes the execution energy and instruction-level energy use by reducing the unnecessary switching activities and making good use of processing resources. The 18 mJ decrease in total energy also shows that the system uses much less energy during its execution and the 100 pJ/instruction lowering in EPI shows better performance at a smaller granularity. The fact that

the two metrics improved by a consistent of 36% is the indicator that the suggested architecture is indeed efficient in optimizing the use of energy and at the same time does not affect performance. Comprehensively, Fig. 5 confirms that the suggested energy-conscious SoC design is able to attain significant improvements in energy efficiency, and, therefore, it is extremely applicable in low-power and sustainable VLSI system design.

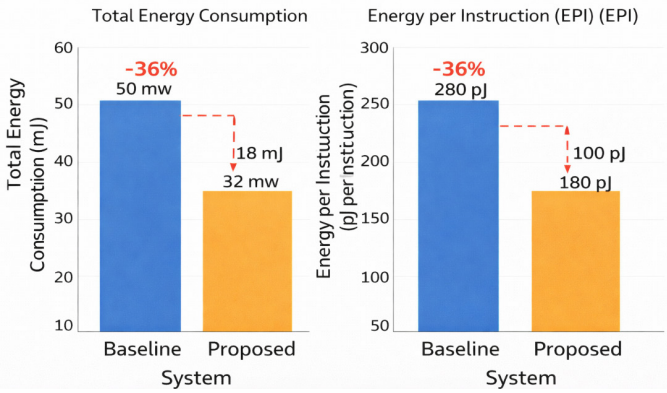

Fig. 5: Comparison of Total Energy Consumption and Energy per Instruction (EPI) Between Baseline and Proposed Energy-Aware SoC Architecture

Performance Impact

The system performance is considered in the context of the impact on latency and throughput. The suggested methodology keeps the performance at competitive levels in the case of aggressive power optimization. There are slight changes in latency brought about by scaling of voltages but these are offset by better resource management and workload distribution. All in all, the system is at a balanced trade-off in the energy savings and computational performance.

Trade-off Evaluation

The Energy-Delay Product (EDP) and Power-Delay Product (PDP) are used to evaluate the trade-off between energy consumption and performance. The given architecture leads to a significant decrease in the EDP and PDP, which suggests that the energy saving is not obtained at the cost of the performance decline. This reaffirms the fact that the combination of DVFS, power gating and adaptive scheduling results in optimal energy-performance tradeoff.

Sustainability Insights

Performance per watt is one of the metrics used to determine the sustainability of the proposed system. The findings demonstrate a significant boost in computational power efficiency in units of power used. Also, low power usage also leads to low thermal generation which increases system reliability and life cycle. Such results prove that the proposed energy-conscious SoC architecture is a good fit to sustain next-generation green VLSI systems.

In general, the experimental findings confirm that the proposed architecture can be effective in minimizing the power consumption, enhancing the energy performance, and preserving the system performance, which makes it a promising solution in terms of energy-efficient and sustainable computing applications.

Conclusion

The paper described a sustainable System-on-Chip (SoC) architecture that incorporates the concept of energy-conscious resource management to tackle the increasing issues of power consumption and energy efficiency in the current VLSI systems. The suggested framework integrates intelligent job scheduling, adaptive resource scheduling, Dynamic Voltage and Frequency Scaling (DVFS) and power gating to balance optimally between performance and energy usage. The design is a holistic solution to energy-efficient computing by including the architectural-level and the circuit-level optimization.

The test outcomes show major positive changes in the main energy consumption and performance indicators. The proposed system results in a reduction of around 29% in total power consumption, reduction of around 36% in total energy consumption and Energy per Instruction (EPI) than baseline systems. Also, the fact that Energy-Delay Product (EDP) and performance per watt have been improved means that the saving of energy is made without reducing the performance of the system. These results confirm the usefulness of incorporating energy-conscious methods in SoC design.

In conclusion, the proposed approach highlights the importance of sustainable design practices in next-generation VLSI systems. The architecture can help in environmentally responsible and scalable computing solutions by decreasing energy use and enhancing efficiency, as well as reducing the thermal impact. The framework is suitable to new uses in embedded systems, IoT, and edge computing where energy efficiency is a fundamental demand.

References

1. Alcala, J. M., Urena, J., Hernandez, A., & Gualda, D. (2017). Sustainable homecare monitoring system by sensing electricity data. *IEEE Sensors Journal*, *17*(23), 7741-7749.
2. Binkert, N., Beckmann, B., Black, G., Reinhardt, S. K., Saidi, A., Basu, A., ... & Wood, D. A. (2011).

The gem5 simulator. *ACM SIGARCH computer architecture news*, *39*(2), 1-7.

3. Bircher, W. L., & John, L. K. (2011). Core-level activity prediction for multicore power management. *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, *1*(3), 218-227.
4. Carlson, T. E., Heirman, W., & Eeckhout, L. (2011, November). Sniper: Exploring the level of abstraction for scalable and accurate parallel multi-core simulation. In *Proceedings of 2011 International Conference for High Performance Computing, Networking, Storage and Analysis* (pp. 1-12).
5. Cicirelli, G., Marani, R., Petitti, A., Milella, A., & D'orazio, T. (2021). Ambient assisted living: a review of technologies, methodologies and future perspectives for healthy aging of population. *Sensors*, *21*(10), 3549.
6. He, J., Zhang, Z., Zhu, L., Zhu, Z., Liu, J., & Gai, K. (2019). An efficient and accurate nonintrusive load monitoring scheme for power consumption. *IEEE Internet of Things Journal*, *6*(5), 9054-9063.
7. Khodayar, M., Wang, J., & Wang, Z. (2019). Energy disaggregation via deep temporal dictionary learning. *IEEE transactions on neural networks and learning systems*, *31*(5), 1696-1709.
8. Kim, Y. G., Kim, M., Kong, J., & Chung, S. W. (2020). An adaptive thermal management framework for heterogeneous multi-core processors. *IEEE Transactions on Computers*, *69*(6), 894-906.
9. Kong, J., Chung, S. W., & Skadron, K. (2012). Recent thermal management techniques for microprocessors. *ACM Computing Surveys (CSUR)*, *44*(3), 1-42.
10. Kumar, P., Lin, Y., Bai, G., Paverd, A., Dong, J. S., & Martin, A. (2019). Smart grid metering networks: A survey on security, privacy and open research issues. *IEEE Communications Surveys & Tutorials*, *21*(3), 2886-2927.
11. Miller, J. E., Kasture, H., Kurian, G., Gruenwald, C., Beckmann, N., Celio, C., ... & Agarwal, A. (2010, January). Graphite: A distributed parallel simulator for multicores. In *HPCA-16 2010 The Sixteenth International Symposium on High-Performance Computer Architecture* (pp. 1-12). IEEE.
12. Ruano, A., Hernandez, A., Ureña, J., Ruano, M., & Garcia, J. (2019). NILM techniques for intelligent home energy management and ambient assisted living: A review. *Energies*, *12*(11), 2203.
13. Shokry, M., Awad, A. I., Abd-Ellah, M. K., & Khalaf, A. A. (2022). Systematic survey of advanced metering infrastructure security: Vulnerabilities, attacks, countermeasures, and future vision. *Future Generation Computer Systems*, *136*, 358-377.
14. Wang, Y., Pandharipande, A., & Fuhrmann, P. (2018). Energy data analytics for nonintrusive lighting asset monitoring and energy disaggregation. *IEEE Sensors Journal*, *18*(7), 2934-2943.